Engineering and Technical Services for Joint Group on Acquisition Pollution Prevention (JG-APP)

Joint Test Protocol
CC-P-1-1

for Validation of Alternatives to Lead-Containing Surface Finishes, for Development of Guidelines for Conformal Coating Usage, and for Qualification of Low-VOC Conformal Coatings

March 11, 1998
(Revised June 23, 1999)

Contract No. DAAA21-93-C-0046
Task No. N.072
CDRL No. A005

Prepared by
National Defense Center for Environmental Excellence (NDCEE)

Operated by Concurrent Technologies Corporation

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PREFACE

This report was prepared by Concurrent Technologies Corporation (*CTC*) through the National Defense Center for Environmental Excellence (NDCEE) under Contract Number DAAA21-93-C-0046. This report was prepared on behalf of, and under guidance provided by, the Joint Group on Acquisition Pollution Prevention (JG-APP) through the Joint Pollution Prevention Advisory Board (JPPAB). The structure, format, and depth of the report's technical content were determined by JPPAB, government technical representatives, and government contractors in response to the specific needs of this project.

THIS REVISED JOINT TEST PROTOCOL (JTP) REFLECTS CLARIFICATIONS TO THE EXECUTION OF THE TESTING PROCEDURES DISCUSSED IN THE PREVIOUS VERSION OF THE JTP DATED MARCH 11, 1998. THESE CLARIFCATIONS ARE DISCUSSED BELOW AND ARE HIGHLIGHTED BY THE REVISION MARKS IN THE BORDER OF THE MODIFIED PAGES OF THE DOCUMENT. NO OTHER CHANGES HAVE BEEN MADE.

JTP Section No.	Original Test Procedure	Modification to Procedure	Rationale
3.3.1 - High Current, Low Voltage (HCLV)	Acceptance criteria of $\Delta V < 0.13$ V	Acceptance criteria of $\Delta V < 0.50$ V	The revision is needed to address the differences in the CCAMTF Automated Test Set (ATS) relative to the manual testing done by the Low-Residue Soldering Task Force (LRSTF).
3.3.5 - High Frequency (HF) Transmission Line Coupler (TLC)	Acceptance criteria of ± 5 dB response for HF TLC 50 MHz, 500 MHz, and 1 GHz	Acceptance criteria of ± 5 dB applied on a PWA-to-PWA basis from the current test time to the pre-test for HF TLC 50 MHz, 500 MHz, and 1 GHz	The changes are needed to correct an apparent oversight in the original JTP that ignored both the original LRSTF criteria for these responses and the effect of the different electrical properties for conformal coating types.
	Acceptance criteria of ± 5 dB response for HF TLC reverse null response	Acceptance criteria of ± 5 dB applied on a PWA-to-PWA basis from the current test time to the pre-test if the pre-test and current measurements are both greater than –50dB; or ± 10 dB applied on a PWA-to-PWA basis from the current test time to the pre-test if either the pre-test measurement or current measurement are less than -50dB for HF TLC reverse null response	
	Acceptance criteria of ± 50 MHz response for HF TLC reverse null frequency	Acceptance criteria of ± 50 MHz applied on a PWA-to-PWA basis from the current test time to the pre-test for HF TLC reverse null frequency	
4.1.1 - Coating Adhesion	Perform the tests on parylene and silicone conformal coatings	Perform the tests on on parylene, urethane, and silicone conformal coatings	The change is necessary to reflect the prior agreement of the technical representatives to test the urethane coating, which was inadvertently omitted from this test procedure.
	Subject the conformal coatings to the following tests: fluid exposure – diesel fuel test, fluid exposure - hydraulic fluid test, vibration test, and mechanical shock test	Subject the conformal coatings to the following tests: fluid exposure – diesel fuel test, hydraulic fluid test, accelerated life test, vibration test, the mechanical shock test, branch water test, and salt fog test	The change is necessary to reflect the prior agreement of the technical representatives to also conduct accelerated life, branch water, and salt fog tests, which were inadvertently omitted from the test procedure. In addition, it was agreed that the hydraulic fluid test would replace the fluid exposure - hydraulic test.

Invaluable technical, business, and programmatic contributions were provided by the organizations listed below.

- AF Corrosion Program Office
- AIM-9X Program Office
- HQ AMCOM
- AMRAAM Program Office
- AMSAM-DSA-SH-PTC
- ASC/EME, Wright Patterson AFB
- Avenger Program Office
- C-17 Program Office
- Office of Chief of Naval Operations, Environmental Protection, Safety, and Occupational Health
- Circuit Card Assembly and Materials Task Force (CCAMTF)
- Defense Contract Management District - West (DCMDW-OS)
- HQ Defense Contract Management Command (DCMC)
- ESC/EN-IB, Hanscom AFB, MA
- F-15 Program Office
- F-16 Program Office
- F-22 Program Office
- HQ-AFMC/LG-EV, Wright Patterson AFB
- Javelin Program Office
- Joint Depot Environmental Panel (JDEP)
- JSOW Program Office
- WR-ALC/LFEFA, Robins AFB
- M1 Abrams Program Office
- MACOM
- NASA Aerospace Materials Division
- Naval Air Warfare Center (NAWC) – Weapons Division
- Naval Surface Warfare Center (NSWC) - Crane Division
- U.S. Army PEO-TAD
- Phalanx Program Office
- RAM Program Office
- Robisan Laboratory, Incorporated
- SHORAD
- Sidewinder Program Office
- Standard Missile Program Office
- Stinger Program Office
- Tank-Automotive and Armament Command (TACOM) – Army Armament Research and Development Energy Center
- Tomahawk Program Office
- Trident Program Office
- U.S. Army HQ-CECOM
- Volcano Program Office
- Warner Robins Air Logistics Center, Robins AFB
- Wright Laboratories, Wright Patterson AFB

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1. INTRODUCTION

On September 15, 1994, the Joint Logistics Commanders (JLC) chartered the Joint Group on Acquisition Pollution Prevention (JG-APP) to coordinate joint service activities affecting pollution prevention issues identified during a defense system's acquisition process. JG-APP's primary objectives are to:

- Reduce or eliminate the use of hazardous materials (HazMats) by fostering joint cooperation
- Avoid duplication of efforts in actions required to reduce or eliminate HazMats and share technology.

JG-APP focuses on implementing pollution prevention processes at defense contractor design, manufacturing, and re-manufacturing locations, with subsequent technology transfer to the U. S. Department of Defense (DoD) Sustainment Community. JG-APP is managed by the Joint Pollution Prevention Advisory Board (JPPAB).

JPPAB, with assistance from the National Defense Center for Environmental Excellence (NDCEE), operated by Concurrent Technologies Corporation (*CTC*) of Johnstown, Pennsylvania, has developed a methodology for implementing pollution prevention processes through interactions with original equipment manufacturers (OEMs) at several defense contractor locations. The JG-APP methodology is being used by the Circuit Card Assembly and Materials Task Force (CCAMTF), with the intent of facilitating the CCAMTF's efforts to identify and use environmentally acceptable materials and processes for circuit card manufacturing and maintenance.

1.1. CCAMTF Overview

The CCAMTF is a consortium of industry, military, and government organizations whose purpose is to identify alternative materials and processes that have the potential to abate environmental, safety, and occupational health (ESOH) risks; reduce costs; and improve efficiency when compared to current methods of circuit card manufacturing and maintenance. Appendix A lists the organizations and their representatives that participate in the CCAMTF.

The CCAMTF is currently implementing initiatives that have significant potential to provide pollution prevention, cost, and production efficiency benefits. These initiatives include:

- Demonstrating and validating lead-free organic and metallic surface finishes
- Developing guidelines for intelligent use of conformal coatings
- Demonstrating and validating low volatile organic compound (VOC) conformal coatings.

Surface finishes containing tin and lead are applied to circuit cards to prevent oxidation of exposed copper. This application ensures a solderable surface when components are added during later stages of processing. The most widely used processes for applying surface finishes are hot-air solder leveling (HASL) with solder mask, and reflowed tin-lead. Both processes generate lead emissions and waste. Lead is a toxic substance that is heavily regulated by various federal, state, and local environmental agencies.

A related concern for fused tin-lead surface finishes is their inability to provide a level soldering surface. Planarity is extremely important in the reliable placement and soldering of fine pitch components. Tin-lead surface finishing is seen as a limiting technology in this respect. The CCAMTF believes that lead-free alternative surface finishes would provide increased planarity.

Conformal coatings are thin layers of synthetic resins or polymers applied to circuit cards for protection against a variety of environmental, mechanical, electrical, and chemical conditions; these conditions include humidity, moisture, contamination, stress, mechanical shock, vibration, thermal cycling, and corrosion. The application process is expensive, and time consuming, and also accounts for up to 40% of the VOC emissions generated from high-volume circuit card manufacturing. (The remaining 60% of VOC emissions is generated by soldering fluxes, primers, and cleaning agents.) VOC emissions are heavily regulated by various federal, state, and local environmental agencies.

The CCAMTF believes that intelligent use of conformal coatings would decrease manufacturing costs, simplify rework, and reduce pollution at the source without degrading circuit card quality or performance. Guidelines for intelligent use of conformal coatings would describe suitable applications that reduce the use of conformal coatings, use low-VOC conformal coatings, or use conformal coatings without primers.

1.2. JG-APP/CCAMTF Interaction

A joint group, led by JPPAB, CCAMTF, and NDCEE/*CTC*, identified engineering, performance, and operational impact (supportability) requirements for circuit cards prepared both with and without conformal coatings, and with various lead-free surface finishes. The joint group consisted of technical representatives from the affected defense programs, DoD Sustainment Community, and other government and contractor organizations. The joint group reached consensus regarding tests to qualify alternatives against the requirements, including procedures, methodologies and acceptance criteria.

This Joint Test Protocol (JTP) contains the critical technical and performance requirements and tests agreed to by the joint group for use on DoD circuit cards.

These requirements are necessary to validate the performance and reliability of circuit card assemblies both with and without conformal coatings, and with lead-free surface finishes. This JTP is also intended to provide guidance to DoD electrical designers for possible elimination of conformal coatings in specific circuit card applications. However, the scope of this JTP is limited to circuit cards that:

- Have electroplated, or rolled, annealed copper circuits on organic laminates
- Are specifically intended for attachment using molten solder either by hand, wave, or reflow soldering
- Contain either surface mount or pin-in-hole components that will be soldered to the circuit card.

A subsequent Joint Test Report (JTR) will document the data and results of testing. The JTP and JTR will be made available to other government and commercial users for guidance on future pollution prevention efforts. Engineering authorities can refer to the conformal coating and lead-free surface finish test results during design decisions for specific defense systems. However, the tests and criteria defined in this JTP were developed by consensus only for the defense system programs involved, and may not address all areas of application.

Table 1 is a summary table which shows the target HazMats, current processes, applications, current specifications, and the defense system programs potentially affected by this CCAMTF/JG-APP project.

Table 1. Target HazMat Summary

Target Hazmats	**Current Processes**	**Applications**
Lead	Surface Finishing	Oxidation Protection
VOCs	Conformal Coating	Corrosion Protection, Electrical Insulation, and Foreign Object Debris (FOD) Protection

Current Specifications			
ANSI/J-STD-001	IPC-D-249	MIL-I-46058	MIL-STD-454
IPC-6011	IPC-D-275	MIL-P-50884	MIL-STD-2000
IPC-6012	IPC-SM-782	MIL-P-55110	MIL-STD-2000A
IPC-2221	IPC-RB-276	MIL-PRF-31032	MIL-STD-2118
IPC-2222	IPC-RF-245	MIL-S-45743	WS6536
IPC-CC-830	MIL-C-28809	MIL-STD-275	
IPC-CM-770			

(Table 1 continued on next page)

Table 1. Target HazMat Summary (Continued)

Potentially Affected Defense Systems
Air Force
AGM-65 Maverick Missile System
APQ-181 (B-2 Radar)
B-2 Spirit Bomber Aircraft
C-17 Globemaster III Transport Aircraft
C130J Hercules Transport Aircraft
C-141B Starlifter Transport Aircraft
Design, Evaluation for Personnel, Training, and Human Factors (DEPTH)
F-15 Eagle Fighter Aircraft
F-16 Fighting Falcon Fighter Aircraft
F-22 Air Superiority Fighter Aircraft
GBU-15 Glide Bomb
High Power Microwave Suppression of Enemy Air Defenses (HPM SEAD)
KC-10A Extender Tanker Aircraft
Solid-State Phased Array (SPAR) Radar System
Army
Advanced Tank Armament System (ATAS)
Avenger Missile System
CH-47 Chinook Transport Helicopter
Cobra-NITE/LAAT Targeting System
FIREFINDER Position Analysis System
Gunner's Primary Sight-Line of Sight (GPSLOS)
Horizontal Technology Integration (HTI) Targeting System
Improved Bradley Acquisition System (IBAS) Targeting System
Improved Target Acquisition System (ITAS) Targeting System
Javelin Missile System
Lightweight Exo-Atmospheric Projectile (LEAP)
M1A2 Abrams MBT CITV/HTEU
M65 TOW Targeting System
M139 VOLCANO Mine Dispensing System
M732A2 Fuze
M762 Fuze
M773 MOFA Fuze
OH-58 Kiowa Transport Helicopter
PALADIN Howitzer Fire Control
Stinger Missile System
Standard Vehicle Mounted Launcher (SVML)
Target Acquisition Designation Sight/Pilot Night Vision Sensor (TADS/PNVS)
TOW 2A & 2B Missile Systems
XM943 Smart Target Activated Fire and Forget (STAFF) Tank Ammunition Round

(Table 1 continued on next page)

Table 1. Target HazMat Summary (Continued)

Navy
AGM-84E SLAM Missile System
APG-73 Radar System
AV-8 Harrier VTOL Attack Aircraft
CIWS Phalanx Weapon System
Evolved SeaSparrow Missile (ESSM) Missile System
F/A-18 Hornet Fighter/Attack Aircraft
Guided Missile Launching System (GMLS)
HH-60 Seahawk Helicopter
Mk612 Standard Missile Test Set
P-3 Orion Synthetic Aperture Radar (SAR)
Rolling Airframe Missile (RAM)
SH-60F CV-Helo ASW Helicopter
SLBM Trident I-C4 & II D-5 Missile System
SM-1, SM-1A & SM-2 Standard Missile Systems
Tomahawk Baseline Improvement Program (TBIP)
Tomahawk Missile System
Joint/Multi-Service Systems
AGM-84D Harpoon Missile System
AIM-9X Sidewinder Missile System
AIM-120 AMRAAM Missile System
AGM-88 HARM Missile System
F-3 Tornado Fighter Aircraft
Integrated Targeting System Gun Management System (ITSGMS)
Joint Air To Surface Standoff Missile (JASSM)
Joint Stand-Off Weapon (JSOW) Missile System
Joint Strike Fighter (JSF) Fighter Aircraft
LAMPS/FLIR Targeting Systems
LANTIRN Targeting System
Objective Individual Combat Weapons (OICW) Weapon System
Outrider Tactical Unmanned Air Vehicle (TUAV)
Paveway III Missile System
V-22 Osprey VTOL Transport Aircraft

2. ENGINEERING AND TESTING REQUIREMENTS

This section summarizes the engineering and testing requirements for circuit cards prepared both with and without conformal coatings, and with various lead-free surface finishes. Tests contained in this JTP may involve the use of hazardous materials. However, this JTP does not address safety issues associated with their use. Therefore, when performing tests described in this JTP, appropriate safety and health practices must be established, and the applicability of regulatory limitations must be determined.

2.1. Test Specimens

Eight test specimen types have been selected for testing:

- Printed wiring assembly (PWA)
- Modified IPC-B-24 board
- MIL-I-46058C Y-coupon
- IPC-B-25 board
- Aluminum alloy 2024 panels
- Glass slides
- Glass fiber (GF) laminate strips
- Surface finish coupon.

2.1.1. Printed Wiring Assembly (PWA)

The printed wiring assembly (PWA) is a test circuit assembly used to evaluate a variety of electrical performance parameters. It was designed to represent the majority of parts produced for military applications, and to accurately reflect relative differences in alternative surface finish and conformal coating performance. The PWA measures 6.05 inches by 5.8 inches by 0.062 inches, and contains the following six sections:

- High current, low voltage (HCLV)
- High voltage, low current (HVLC)
- High speed digital (HSD)
- High frequency (HF)
    - Other networks (ON)
- Stranded wire (SW).

Each section of the PWA has independently performing subsections for plated through hole (PTH) and surface mount technology (SMT) components. Each subsection (except the SW section) contains both functional and nonfunctional components (added to increase component density). A 29-pin PTH edge connector is used for circuit testing. High

frequency connectors are used to ensure proper impedance matching and test signal fidelity. Two stranded wires are soldered to terminals on the board. The PWA includes a common ground plane, components with heat sinks, and mounted hardware. Appendix B contains a detailed description of the Low-Residue Soldering Task Force (LRSTF) PWA.

2.1.2. Modified IPC-B-24 Board

The standard IPC-B-24 board is a test board used to evaluate the interaction of flux and paste residues (described in the *Institute for Interconnecting and Packaging Electronic Circuits Surface Insulation Resistance Handbook (IPC-9201)*, October 1992). On the modified IPC-B-24 board, the standard 20 mil comb pattern spacing is changed on three of the four comb patterns to 16 mil, 12 mil, and 8 mil. Figures 1 and 2 below illustrate the configuration of an IPC-B-24 board and the modified IPC-B-24 board, respectively.

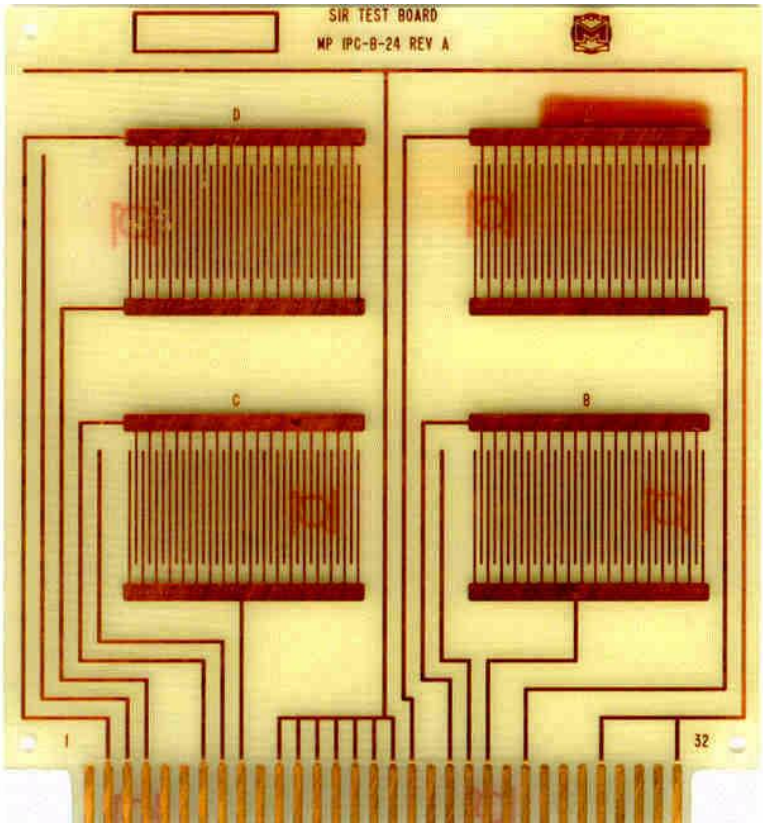


Figure 1. IPC B-24 Board

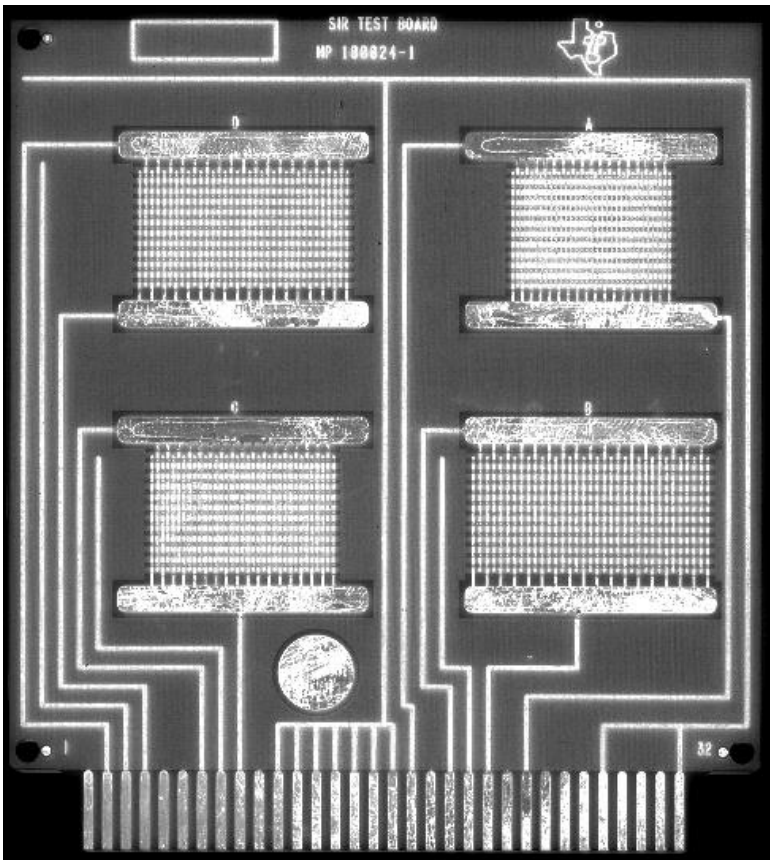


Figure 2. Modified IPC-B-24 Board

2.1.3. MIL-I-46058C Y-Coupon

The MIL-I-46058C Y-Coupon, (described in paragraph. 4.7.1.1 of *Insulating Compound, Electrical For Coating Printed Wire Assemblies*, September 1993) is a test coupon used to evaluate conformal coating and alternative surface finish performance. It is fabricated from single-sided, copper clad, glass-epoxy laminate. Figure 3 depicts the configuration of a MIL-I-46058C Y- Coupon.

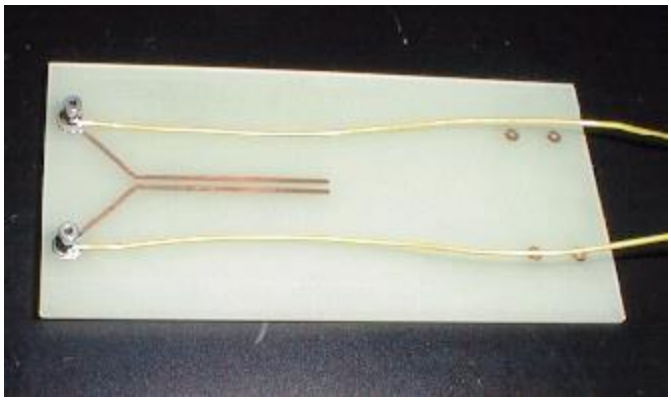


Figure 3. MIL-I-46058 Y Coupon

When used specifically for evaluating conformal coating materials, the copper cladding is 2 ounces thick. When used for the evaluating surface finishes, either 0.5 or 1.0 ounce foils may be used for the base copper, as they will all have at least 0.001 inch electroplated copper applied to the surface, simulating the "as-received condition" of the PWAs.

2.1.4. IPC-B-25 Board

The standard IPC-B-25 board is a test board used to evaluate electromigration. It is constructed in accordance with IPC-TR-476 (described in Institute for Interconnecting and Packaging Electronic Circuits, *How to Avoid Metallic Growth Problems on Electronic Hardware*, 1977). Figure 4 depicts the configuration of an IPC-B-25 board.

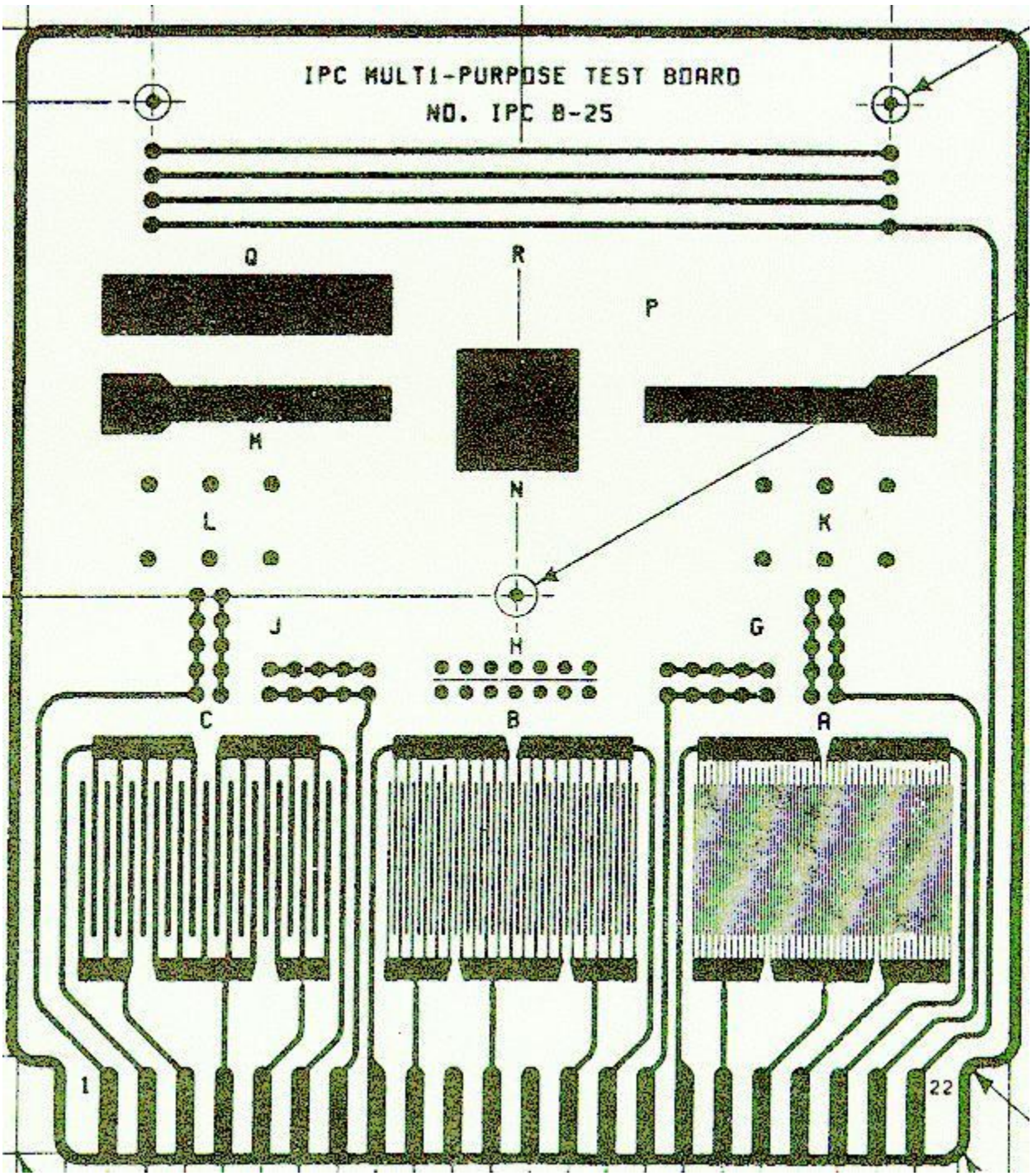


Figure 4. IPC-B-25 Board

2.1.5. Aluminum Alloy 2024 Test Panel

The aluminum alloy 2024 test panel is used to evaluate applied coating thickness and coating flexibility. A test panel is fabricated from aluminum alloy 2024 sheet metal and measures 3 inches by 6 inches by 0.032 inch.

2.1.6. Glass Slide

A standard glass microscope slide is used to evaluate fungus resistance. A standard glass slide measures 25 millimeter by 75 millimeter by 1 millimeter.

2.1.7. Glass Fiber (GF) Laminate Strip

A glass-fiber (GF) laminate strip is a test specimen used to evaluate flame resistance and coating adhesion. A GF strip measures 5 inches by 3 inches and is fabricated from 2-ounce, single-sided, copper- clad, glass-epoxy laminate in accordance with MIL-I-46058C (described in *Insulating Compound, Electrical, For Coating Printed Circuit Assemblies*, September 1993).

2.1.8. Surface-Finish Coupon

A surface-finish coupon is a test specimen used to evaluate alternative surface finishes. A surface finish coupon is fabricated from copper and measures 2 inches by 1 inch by 0.027 inch.

2.2. Automated Test Set (ATS)

The CCAMTF automated test set (ATS) is a conventional rack-and-stack type test set used to test various electrical performance parameters of the PWA as described in Section 2.1.1. The test set consists of a two-bay equipment cabinet, commercially available test equipment, a test fixture, computer, associated wiring, cable harnesses, and RF type coaxial cables. All commercial test equipment used is controlled by the general-purpose interface bus (GPIB, IEEE 488 standard). Appendix F provides a further description and figure of the ATS.

2.3. Alternative Surface Finish (ASF) Screening Test Summary

Alternative surface finish screening tests are initial tests used to evaluate several critical properties of alternative surface finishes. These tests will reveal those finishes that do not meet the acceptance criteria of the tests. Table 2 summarizes the alternative surface finish screening tests.

Table 2. Alternative Surface Finish Screening Tests

Screening Test	JTP Section	Reference	Acceptance Criteria
Surface Insulation Resistance (SIR)	3.1.1	IPC-TM-650, Method 2.6.3.3	$\geq 10^8\ \Omega$
Electromigration	3.1.2	IPC-TM-650, Method 2.6.14	$\geq 10^5\ \Omega$
Solderability	3.1.3	ANSI/J-STD-003	Force at 2 seconds ≥ hot-air solder leveling (HASL) baseline surface finish performance
Contamination Characterization (Extended Test)[a]	3.1.4	IPC-TM-650, Method 2.3.28	Low-residue flux finished assemblies: (expected contamination) • $Cl^- < 2.5\ \mu g/in^2$ • $Br^- < 15\ \mu g/in^2$ Water-soluble flux finished assemblies: (expected contamination) • $Cl^- < 4.5\ \mu g/in^2$ • $Br^- < 15\ \mu g/in^2$

[a] The contamination characterization test is not required by all defense system programs, and is therefore known as an "extended test." The test may be performed at the discretion of each specific defense system program.

2.4. Conformal Coating Screening Test Summary

Conformal coating screening tests are initial tests used to evaluate several critical properties of conformal coatings. These tests will reveal those coatings that do not meet the acceptance criteria of the tests. In some instances, one test, such as a dielectric withstanding voltage test, supports another test, such as thermal shock test, to define acceptance criteria. The dielectric withstanding voltage test would be considered the "supporting test" in this case. Table 3 summarizes the conformal coating screening tests.

Table 3. Conformal Coating Screening Tests

Screening Test	JTP Section	Reference	Supporting Test	JTP Section	Acceptance Criteria
Coating Thickness	3.2.1	ASTM D 1005-95	Not Applicable	Not Applicable	Acrylic resin, epoxy resin, and urethane resin: 0.002 ± 0.001 inch Silicone resin: 0.005 ± 0.003 inch Parylene: 0.0005 to 0.0020 inch
Fungus Resistance	3.2.2	ASTM G 21-90	Not Applicable	Not Applicable	Rating of 0
Flexibility	3.2.3	FED-STD-141C, Method 6221	Not Applicable	Not Applicable	No cracking or crazing
Flame Resistance	3.2.4	ASTM D 635-91	Not Applicable	Not Applicable	Self-extinguishing or non-burning
Resonance	3.2.5	Not Applicable	Not Applicable	Not Applicable	The minimum Q value for uncoated type GF laminates at frequencies of 1 and 50 MHz shall be 50 and 70, respectively.[a]
Thermal Shock	3.2.6	Not Applicable	Dielectric Withstanding Voltage	3.2.7	≤ 10 μA
Dielectric Withstanding Voltage	3.2.7	Not Applicable	Not Applicable	Not Applicable	≤ 10 μA

[a] See Section 3.2.7 of this document for the maximum allowable changes due to the application of coatings.
[b] The supporting adhesion test can be referenced in ASTM D 3359-95a.

(Table 3 continued on next page)

Table 3. Conformal Coating Screening Tests (Continued)

Screening Test	JTP Section	Reference	Supporting Test	JTP Section	Acceptance Criteria
Insulation Resistance	3.2.8	Not Applicable	Not Applicable	Not Applicable	Each specimen ≥ 1.5 X 10^{12} Ω Average specimen ≥ 2.5 X 10^{12} Ω
Moisture Resistance	3.2.9	Not Applicable	Dielectric Withstanding Voltage	3.2.7	≤ 10 μA
			Insulation Resistance	3.2.8	Each acrylic resin, silicone resin, urethane resin, parylene ≥ 5.0 X 10^{9} Ω Each epoxy resin ≥ 5.0 X 10^{8} Ω Average acrylic resin, silicone resin, urethane resin, parylene ≥ 1.0 X 10^{10} Ω Average epoxy resin ≥ 1.0 X 10^{9} Ω
Thermal Humidity Aging	3.2.10	Not Applicable	Not Applicable	Not Applicable	No evidence of reversion No loss of legibility
			Adhesion[b]	3.2.11	Rating ≥ 4
Adhesion	3.2.11	ASTM D 3359-95a	Not Applicable	Not Applicable	Rating ≥ 4

[a] See Section 3.2.7 of this document for the maximum allowable changes due to the application of coatings.
[b] The supporting adhesion test can be referenced in ASTM D 3359-95a.

2.5. Summary of Environmental Exposure Validation, Physical Reliability Validation, and Electrical Performance Tests

Alternative surface finishes and conformal coatings that meet the acceptance criteria of their respective screening tests will then be subjected to validation tests. As applicable, electrical performance of a test specimen will be tested prior to, during, and after each validation test. Tables 4 and 5 summarize the environmental exposure and physical reliability validation tests, along with their accompanying electrical performance tests.

Table 4. Environmental Exposure Validation Tests

Validation Test	JTP Section	Reference	Electrical Performance Test[a]	JTP Section	Acceptance Criteria[b]
Environmental 85°C/85% Relative Humidity (RH)	3.4.1	IPC-TM-650, Method 2.6.3.3 MIL-PRF-38535D	HCLV	3.3.1	$\Delta V < 0.50$ V
			HVLC	3.3.2	4 to 6 μA
			HSD	3.3.3	≤ 20% increase in propagation delay time from baseline
			HF	3.3.4	See JTP Tables 29 and 30
			ON	3.3.5	$\geq 5 \times 10^7$ Ω
			SW	3.3.6	$\Delta V < 0.356$ V
Condensing Atmosphere	3.4.2	MIL-STD-883E, Method 1004.7	HCLV	3.3.1	$\Delta V < 0.50$ V
			HVLC	3.3.2	4 to 6 μA
			HSD	3.3.3	≤ 20% increase in propagation delay time from baseline
			HF	3.3.4	See JTP Tables 29 and 30
			ON	3.3.5	$\geq 5 \times 10^7$ Ω
			SW	3.3.6	$\Delta V < 0.356$ V
Fluid Exposure - Diesel Fuel	3.4.3	SAE J1211	HCLV	3.3.1	$\Delta V < 0.50$ V
			HVLC	3.3.2	4 to 6 μA
			HSD	3.3.3	≤ 20% increase in propagation delay time from baseline
			HF	3.3.4	See JTP Tables 29 and 30
			ON	3.3.5	$\geq 5 \times 10^7$ Ω
			SW	3.3.6	$\Delta V < 0.356$ V

[a] HCLV = high current, low voltage; HF = high frequency
HVLC = high voltage, low current; ON = other networks
HSD = high speed digital; SW = stranded wire

[b] Failure of a test board in a specific test does not necessarily disqualify a conformal coating process or alternative surface finish for use in an application for which that test does not apply. Electrical performance requirements for a particular circuit apply only to parts containing that circuit.

(Table 4 continued on next page)

Table 4. Environmental Exposure Validation Tests (Continued)

Validation Test	JTP Section	Reference	Electrical Performance Test[a]	JTP Section	Acceptance Criteria[b]
Fluid Exposure - Hydraulic Fluid	3.4.4	SAE J1211	HCLV	3.3.1	$\Delta V < 0.50$ V
			HVLC	3.3.2	4 to 6 μA
			HSD	3.3.3	≤ 20% increase in propagation delay time from baseline
			HF	3.3.4	See JTP Tables 29 and 30
			ON	3.3.5	$\geq 5 \times 10^7\ \Omega$
			SW	3.3.6	$\Delta V < 0.356$ V
Branch Water Test (Condensed Moisture Test)	3.4.5	Not Applicable	HCLV	3.3.1	$\Delta V < 0.50$ V
			HVLC	3.3.2	4 to 6 μA
			HSD	3.3.3	≤ 20% increase in propagation delay time from baseline
			HF	3.3.4	See JTP Tables 29 and 30
			ON	3.3.5	$\geq 5 \times 10^7\ \Omega$
			SW	3.3.6	$\Delta V < 0.356$ V

[a] HCLV = high current, low voltage; HF = high frequency
HVLC = high voltage, low current; ON = other networks
HSD = high speed digital; SW = stranded wire

[b] Failure of a test board in a specific test does not necessarily disqualify a conformal coating process or alternative surface finish for use in an application for which that test does not apply. Electrical performance requirements for a particular circuit apply only to parts containing that circuit.

(Table 4 continued on next page)

Table 4. Environmental Exposure Validation Tests (Continued)

Validation Test	JTP Section	Reference	Electrical Performance Test[a]	JTP Section	Acceptance Criteria[b]
Accelerated Life Test	3.4.6	Not Applicable	HCLV	3.3.1	$\Delta V < 0.50$ V
			HVLC	3.3.2	4 to 6 μA
			HSD	3.3.3	≤ 20% increase in propagation delay time from baseline
			HF	3.3.4	See JTP Tables 29 and 30
			ON	3.3.5	$\geq 5 \times 10^7$ Ω
			SW	3.3.6	$\Delta V < 0.356$ V
Sulfur Dioxide/Salt Fog Resistance	3.4.7	Not Applicable	HCLV	3.3.1	$\Delta V < 0.50$ V
			HVLC	3.3.2	4 to 6 μA
			HSD	3.3.3	≤ 20% increase in propagation delay time from baseline
			HF	3.3.4	See JTP Tables 29 and 30
			ON	3.3.5	$\geq 5 \times 10^7$ Ω
			SW	3.3.6	$\Delta V < 0.356$ V

[a] HCLV = high current, low voltage; HF = high frequency
HVLC = high voltage, low current; ON = other networks
HSD = high speed digital; SW = stranded wire

[b] Failure of a test board in a specific test does not necessarily disqualify a conformal coating process or alternative surface finish for use in an application for which that test does not apply. Electrical performance requirements for a particular circuit apply only to parts containing that circuit.

Table 5. Physical Reliability Validation Tests

Validation Test	JTP Section	Reference	Electrical Performance Test[a]	JTP Section	Acceptance Criteria[b]
Thermal Shock	3.5.1	Not Applicable	HCLV	3.3.1	$\Delta V < 0.50$ V
			HVLC	3.3.2	4 to 6 μA
			HSD	3.3.3	≤ 20% increase in propagation delay time from baseline
			HF	3.3.4	See JTP Tables 29 and 30
			ON	3.3.5	$\geq 5 \times 10^7\ \Omega$
			SW	3.3.6	$\Delta V < 0.356$ V
Thermal Cycling	3.5.2	Not Applicable	HCLV	3.3.1	$\Delta V < 0.50$ V
			HVLC	3.3.2	4 to 6 μA
			HSD	3.3.3	≤ 20% increase in propagation delay time from baseline
			HF	3.3.4	See JTP Tables 29 and 30
			ON	3.3.5	$\geq 5 \times 10^7\ \Omega$
			SW	3.3.6	$\Delta V < 0.356$ V

[a] HCLV = high curent, low voltage; HVLC = high voltage, low current; HSD = high speed digital; HF = high frequency; ON = other networks; SW = stranded wire

[b] Failure of a test board in a specific test does not necessarily disqualify a conformal coating process or alternative surface finish for use in an application for which that test does not apply. Electrical performance requirements for a particular circuit apply only to parts containing that circuit.

(Table 5 continued on next page)

Table 5. Physical Reliability Validation Tests (Continued)

Validation Test	JTP Section	Reference	Electrical Performance Test[a]	JTP Section	Acceptance Criteria[b]
Vibration	3.5.3	Not Applicable	HCLV	3.3.1	$\Delta V < 0.50$ V
			HVLC	3.3.2	4 to 6 μA
			HSD	3.3.3	≤ 20% increase in propagation delay time from baseline
			HF	3.3.4	See JTP Tables 29 and 30
			ON	3.3.5	$\geq 5 \times 10^7\ \Omega$
			SW	3.3.6	$\Delta V < 0.356$ V
Mechanical Shock	3.5.4	Not Applicable	HCLV	3.3.1	$\Delta V < 0.50$ V
			HVLC	3.3.2	4 to 6 μA
			HSD	3.3.3	≤ 20% increase in propagation delay time from baseline
			HF	3.3.4	See JTP Tables 29 and 30
			ON	3.3.5	$\geq 5 \times 10^7\ \Omega$
			SW	3.3.6	$\Delta V < 0.356$ V

[a] HCLV = high current, low voltage; HF = high frequency
HVLC = high voltage, low current; ON = other networks
HSD = high speed digital; SW = stranded wire

[b] Failure of a test board in a specific test does not necessarily disqualify a conformal coating process or alternative surface finish for use in an application for which that test does not apply. Electrical performance requirements for a particular circuit apply only to parts containing that circuit.

2.6. Test Flow

Figures 5 and 6 depict test flow diagrams for screening alternative surface finishes and conformal coatings. Alternative surface finishes and conformal coatings that meet the acceptance criteria of the screening tests will be subsequently validated in accordance with environmental exposure and physical reliability validation tests. Figure 7 depicts the test flow diagram for conducting environmental exposure and physical reliability validation tests.

All tests should be conducted in a manner that will eliminate duplication and maximize use of each test specimen. However, the number and types of tests that can be run on a single specimen may be limited by the destructiveness of the tests.

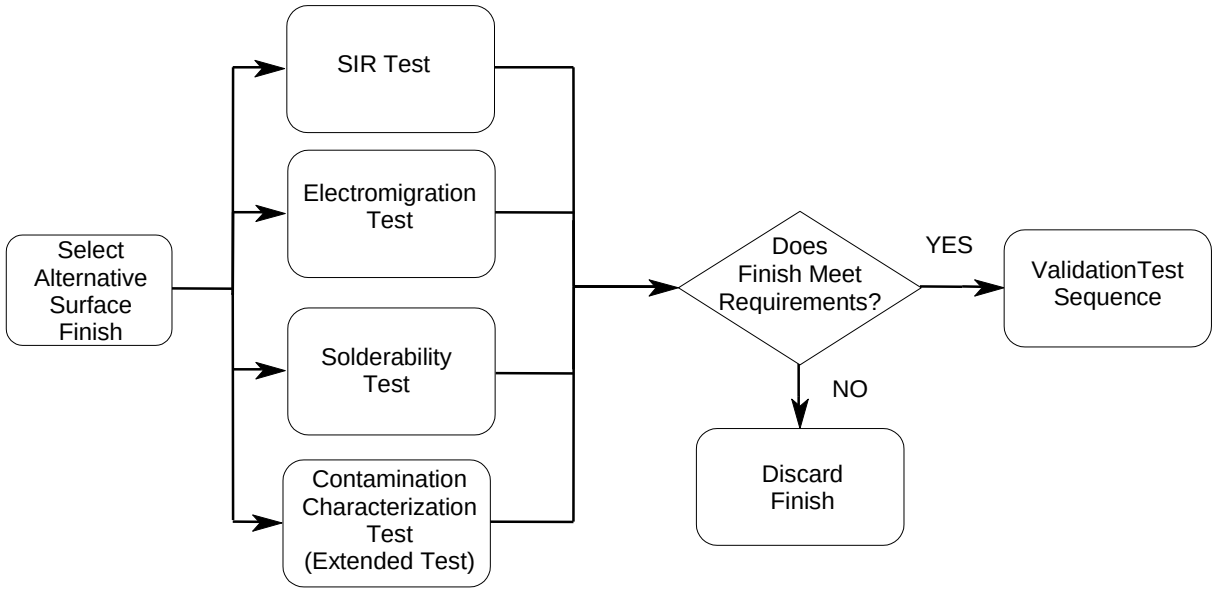


Figure 5. Alternative Surface Finish Screening Test Flow

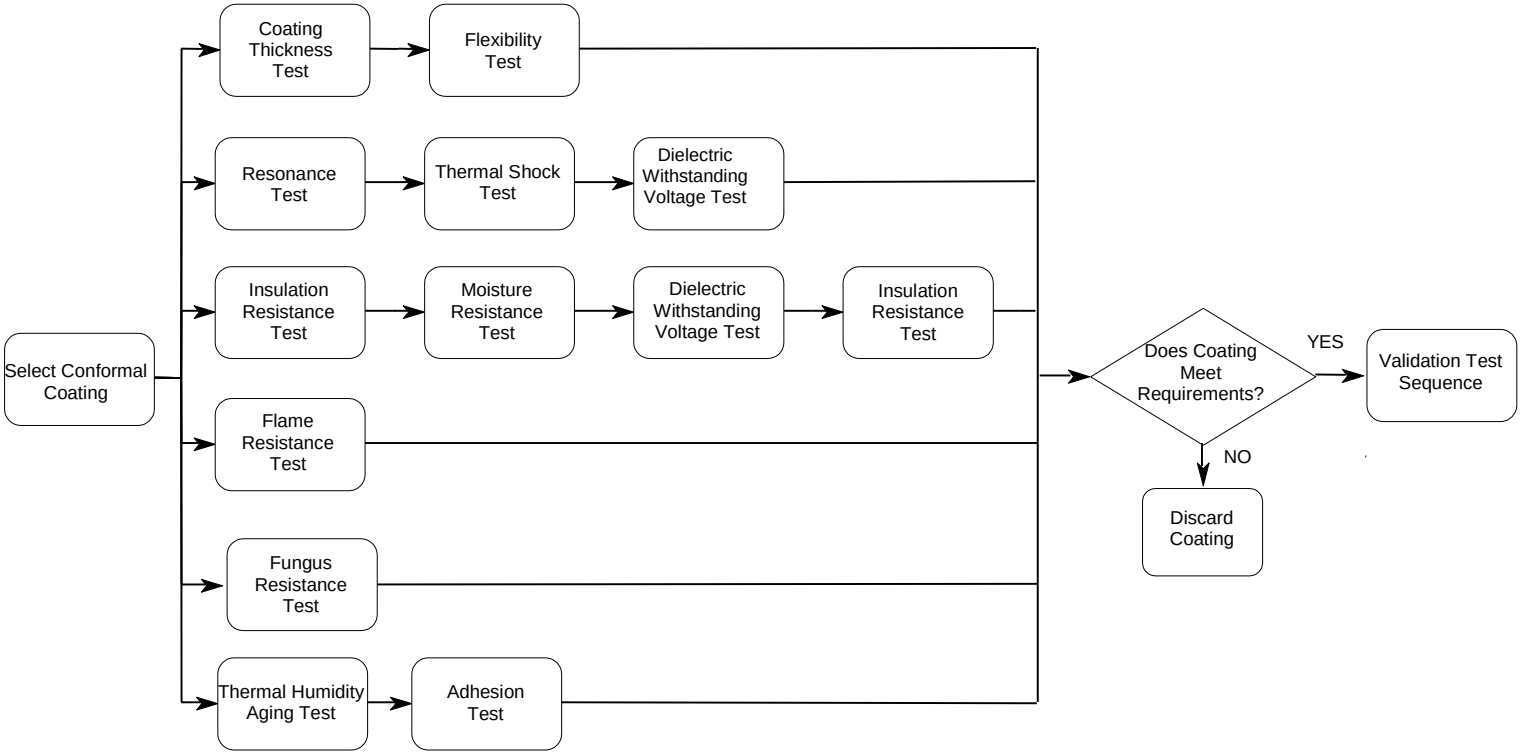
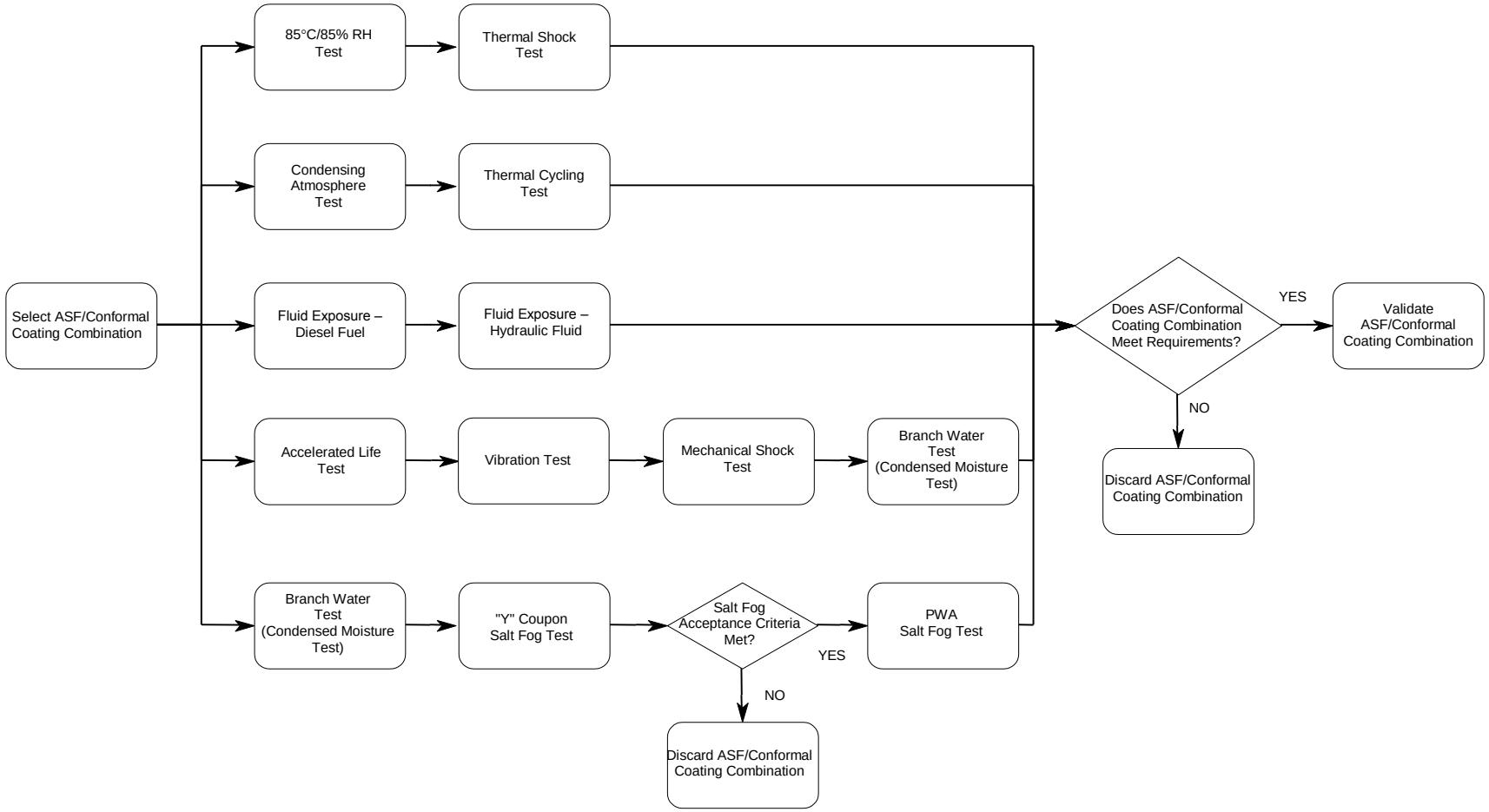


Figure 6. Conformal Coating Screening Test Flow



Note: ASF = alternative surface finish

Figure 7. Validation Test Flow

3. TEST DESCRIPTIONS

Section 3.1 describes each alternative surface finish screening test listed in Table 2 of Section 2.3. Each test includes a description, rationale, and methodology. The methodology includes the parameters, number and type of test specimens per alternative surface finish, number of trials per specimen, and acceptance criteria. When needed, any major or unique equipment, and data recording and calculation requirements are included.

Section 3.2 describes each conformal coating screening test listed in Table 3 of Section 2.4. Each test includes a description, rationale, and methodology. The methodology includes the parameters, number and type of test specimens per conformal coating, number of trials per specimen, and acceptance criteria. When needed, any major or unique equipment, and data recording and calculation requirements are included.

Section 3.3 describes each electrical performance test listed in Tables 4 and 5 of Section 2.5. Each test includes a description, rationale, and methodology. The methodology includes the parameters and acceptance criteria. When needed, any major or unique equipment, and data recording and calculation requirements are included. Electrical performance tests will be conducted prior to, during, and after each environmental exposure and physical reliability validation test.

Sections 3.4 and 3.5 describe each environmental exposure and physical reliability validation test listed in Tables 4 and 5 of Section 2.5. Each test includes a test description, rationale, and test methodology. The test methodology includes the test parameters, number and type of test specimens per alternative surface finish/conformal coating combination, number of trials per specimen, and acceptance criteria. When needed, any major or unique equipment, and data recording and calculation requirements are included.

The information contained in Sections 3.1 to 3.5 is brief and was intended to provide the information needed to understand and perform the tests. These sections can serve as a guide to those performing the tests.

3.1. Alternative Surface Finish Screening Tests

3.1.1. Surface Insulation Resistance (SIR)

Description

This test determines the surface insulation resistance of a test specimen.

Perform this test in accordance with IPC-TM-650, Method 2.6.3.3 (*Institute for Interconnecting and Packaging Electronic Circuits Test Methods Manual*, January 1995). A modified IPC-B-24 board is subjected to elevated levels of temperature and humidity, under an applied voltage potential.

Rationale

SIR testing is an accelerated aging test intended to accelerate electrochemical failure mechanisms that would occur in field service. Failure mechanisms include electrolytic corrosion, electrical leakage, and metal migration (dendritic growth).

Methodology

Table 6. Surface Insulation Resistance Methodology

Parameters	50 V applied bias 100 V testing voltage 85°C 85% relative humidity 168 hours
Number and Type of Specimens	28 modified IPC-B-24 boards per alternative surface finish
Trials per Specimen	1
Acceptance Criteria	$\geq 10^8\ \Omega$

Major or Unique Equipment

- Temperature/humidity chamber
- 50 V DC bias source

Data Recording and Calculations

- Record SIR measurements at the following time intervals:

  - 0 hours
  - 24 hours
  - 96 hours
  - 168 hours
  - 2 hours post
  - 24 hours post

- Document appearance and photograph at 10 times magnification

3.1.2. Electromigration

Description

This test determines the ability of a polymer solder mask coating to withstand an environment conducive to electromigration.

Perform this test in accordance with IPC-TM-650, Method 2.6.14, Revision A (*Institute for Interconnecting and Packaging Electronic Circuits Test Methods Manual, Resistance to Electromigration, Polymer Solder Mask*, August 1987), but with the modifications and additions listed below.

- Solder single-stranded insulated teflon wire to each land of comb pattern C on the 20 modified IPC-B-24 boards. (Ten of the boards should have simulated reflow with a low residue flux.) Wire the combs as shown in Figure 8.
- Solder single-stranded insulated teflon wires to each MIL-I-46058C Y coupon. (Ten of the coupons should have simulated reflow with a low residue flux.) Wire the coupons as shown in Figure 9.

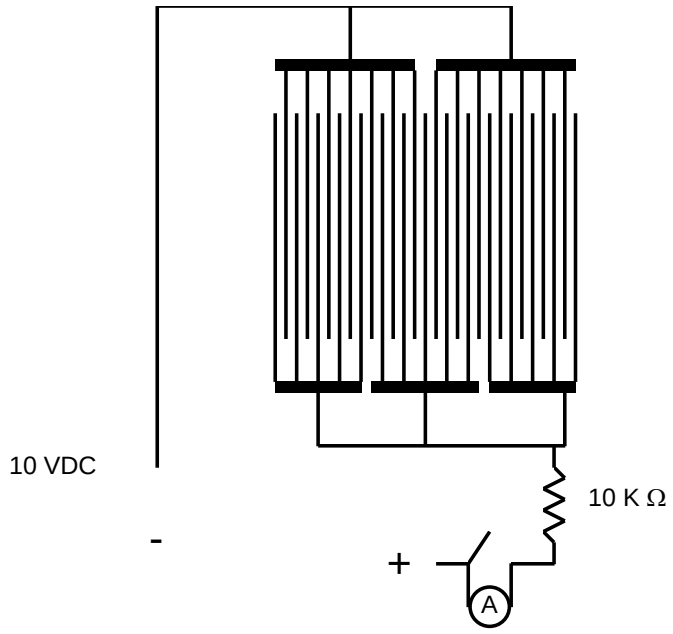


Figure 8. Comb Pattern for Electromigration Testing

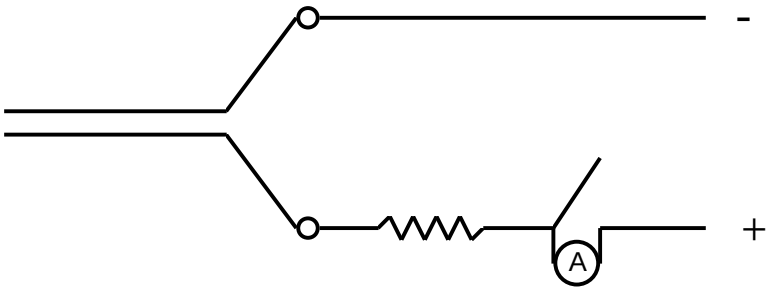


Figure 9. Standard "Y" Pattern Used in Electromigration and Dendritic Growth Testing

- Connect the 12 mil comb to a 10 V DC power supply outside the chamber, with the 10 K Ω limiting resistor in line to limit the current to 1 milliampere.
- Connect the MIL-I-46058C Y coupon to a 10 V DC power supply outside the chamber, with the 10 K Ω limiting resistor in line to limit the current to 1 milliampere.
- Place the test specimens in a humidity chamber at 85°C/ 90% relative humidity in a vertical position such that they do not touch one another.

Rationale

Electromigration testing is an accelerated aging test intended to accelerate electrochemical failure mechanisms that would occur in field service. Failure mechanisms include electrolytic corrosion, electrical leakage, and metal migration (dendritic growth). Electromigration differs from SIR in that a smaller comb pattern is used, therefore simulating a longer exposure time.

*IPC-TM-650, Method 2.6.14, Revision A (*Institute for Interconnecting and Packaging Electronic Circuits Test Methods Manual, Resistance to Electromigration, Polymer Solder Mask*, August 1987) is modified to prevent contamination of the boards. The test as described in the method specifies the use of a desiccator containing a desiccating solution, which poses a contamination potential. The use of a temperature/humidity chamber achieves the required conditions without the desiccating solution, thereby removing the source of contamination.*

Methodology

Table 7. Electromigration Methodology

Parameters	10 V DC applied bias 85°C ± 2°C 90% relative humidity 168 hours
Number and Type of Specimens	10 modified IPC-B-24 boards (after fabrication) per alternative surface finish 10 modified IPC-B-24 boards (after simulated reflow) per alternative surface finish 10 MIL-I-46058 Y coupons (after fabrication) per alternative surface finish 10 MIL-I-46058 Y coupons (after simulated reflow) per alternative surface finish
Trials per Specimen	1
Acceptance Criteria	$\geq 10^5\ \Omega$

Major or Unique Equipment

- Power supply capable of providing a 10 V ± 5% electrical bias @ ≤ 1 amp
- 10 K Ω resistor
- Temperature/humidity chamber capable of 85°C/90% relative humidity.

Data Recording and Calculations

- Visually observe electromigration
- Record current leakage and report in Ω using V=IR for conversion
- Document appearance and photograph at 10 times magnification

3.1.3. Solderability

Description

This test determines the solderability of printed wiring board surface finishes.

Perform this test in accordance with ANSI/J-STD-003, paragraph 4.3.1 (*Solderability Tests for Printed Boards*, April 1992), using the wetting balance and testing the specimens under the following conditions:

- After fabrication, run through the reflow oven in air (simulates a double-sided surface mount or mixed technology process)
- Run through the reflow oven in nitrogen (simulates a double-sided surface mount or mixed technology process)
- Bake in air for eight hours at 105°C and process through the reflow oven in air (simulates a typical bake to remove moisture)
- Bake in nitrogen for eight hours at 105°C and process through the reflow oven in nitrogen (simulates a typical bake to remove moisture)
- Place test specimens in humidity chamber at 50°C/90% relative humidity for 168 hours.

Rationale

In general, components are soldered to circuit card assemblies after surface finishing. The surface finish must be capable of accepting solder.

The exposure conditions simulate typical storage and PWA soldering conditions.

Methodology

Table 8. Solderability Methodology

Parameters	50°C 90% relative humidity 168 hours
Number and Type of Specimens	5 surface finish coupons per alternative surface finish
Trials per Specimen	1
Acceptance Criteria	Force at 2 seconds ≥ 0.100 millinewtons/millimeter (mN/mm)

Major or Unique Equipment

Wetting balance

Data Recording and Calculations

Average wetting force at two seconds

3.1.4. Contamination Characterization

Description

This test determines the level of anionic contaminants on the surface finish of a test specimen. (This test is not required by all defense system programs, and is therefore known as an "extended" test; it may be performed at the discretion of each defense system program.)

Extract a test specimen and perform ion chromatography analysis in accordance with IPC-TM-650, Method 2.3.28 (*Institute for Interconnecting and Packaging Electronic Circuits Test Methods Manual, Ionic Analysis of Circuit Boards, Ion Chromatography Method*, January 1995).

Rationale

Chloride and bromide contents greater than the acceptance criteria levels may correlate to increasing risks of electrolytic failures due to electrical leakage, electrochemical migration, and electrolytic corrosion.

Results of the contamination characterization test will be used to assess the baseline condition of the test specimens prior to assembly soldering and coating.

Methodology

Table 9. Contamination Characterization Methodology

Parameters	Extract: 80°C for 60 minutes
Number and Type of Specimens	48 modified IPC-B-24 boards per alternative surface finish 5 PWAs before assembly processing per alternative surface finish 3 PWAs after soldering processing per alternative surface finish
Trials Per Specimen	1

(Table 9 continued on next page)

Table 9. Contamination Characterization Methodology (Continued)

Acceptance Criteria	Low residue flux finished assemblies: - $Cl^- < 2.5\ \mu g/in^2$ - $Br^- < 15\ \mu g/in^2$ Water-soluble flux finished assemblies: - $Cl^- < 4.5\ \mu g/in^2$ - $Br^- < 15\ \mu g/in^2$

Major or Unique Equipment

- Ion chromatograph with electrolytic conductivity detector
- Kapak bag

Data Recording and Calculations

- Record and report Cl^- and Br^- concentrations
- Calculate the anion contamination as follows:

$$\mu g / in^2 = \frac{(ppb/1000) \times (V_f / V_0)}{A(in^2)}$$

Where V_f = final volume
A = surface area
V_o = original volume

3.2. Conformal Coating Screening Tests

3.2.1. Coating Thickness

Description

This test determines the dry film thickness of a conformal coating film.

Perform this test in accordance with ASTM D 1005-95 (*Measurement of Dry-Film Thickness of Organic Coatings Using Micrometers*, February 15, 1995).

Rationale

This test determines whether a conformal coating material can be applied and dried or cured to a specified film thickness, and if excessive shrinkage occurs during the drying or curing of the material.

This test uses aluminum test specimens in lieu of glass slides to allow subsequent flexibility testing of the conformal coating films.

Methodology

Table 10. Coating Thickness Methodology

Parameters	Apply and cure the specimen according to the manufacturer's curing profile
Number and Type of Specimens	4 aluminum 2024 series alloy panels per conformal coating alternative
Trials per Specimen	1
Acceptance Criteria	• Acrylic resin, epoxy resin, and urethane resin: 0.002 ± 0.001 inch • Silicone resin: 0.005 ± 0.003 inch • Parylene: 0.0005 to 0.0020 inch • No excessive shrinkage

Major or Unique Equipment

Micrometer accurate to 0.0005 inch

Data Recording and Calculations

Cured/dried film thickness

3.2.2. Fungus Resistance

Test Description

This test determines the ability of a conformal coating film to resist fungal growth.

Perform this test in accordance with ASTM G 21-90 (*Standard Practice for Determining Resistance of Synthetic Polymeric Materials to Fungi*, October 26, 1990) using the five fungus types listed in Table 11 for inoculation.

Table 11. Fungus Type

Fungus Type	ATCC[a] No.	MYCO[b] No.
Aspergillus Niger	9642	386
Penicillium Pinophilum[c]	11797	391
Chaetomium Globosum	6205	459
Gliocladium Virens	9645	365
Aureobasidium Pullulans	15233	279

[a] American Type Culture Collection, 12301 Parklawn Drive, Rockville, MD 20852
[b] Mycological Services, Box 1056, Crawfordsville, IN 47933
[c] Historically known as funiculosm

Visually inspect the specimens using 10 times magnification.

Rationale

Fungi can compromise the performance of the conformal coating.

The five fungi selected and listed in Table 11 are representative of common types found throughout the world.

Methodology

Table 12. Fungus Resistance Methodology

Parameters	Incubation: 672 hours (four weeks) at 28°C to 30°C and 85% relative humidity
Number and Type of Specimens	4 glass slides per fungus per conformal coating alternative
Trials per Specimen	1
Acceptance Criteria	Rating of zero (must not support fungus growth)

Major or Unique Equipment

- Incubator capable of 28°C to 30°C and 85% relative humidity
- Microscope
- Fungus cultures
- Nutrient salts

Data Recording and Calculations

Record observed growth on specimens according to Table 13.

Table 13. Fungus Growth Rating

Observed Growth on Specimens	Rating
None	0
Traces of Growth (less than 10%)	1
Light Growth (10% to 30%)	2
Medium Growth (30% to 60%)	3
Heavy Growth (60% to complete coverage)	4

3.2.3. Flexibility

Test Description

This test determines the flexibility of a conformal coating film.

Perform this test in accordance with FED-STD-141C, Method 6221 (*Paint, Varnish, and Related Materials: Methods of Inspection, Sampling, and Testing*, January 24, 1986).

Rationale

Conformal coating films may be subjected to flexion stresses. This test evaluates the performance of a film under such stresses.

Methodology

Table 14. Flexibility Methodology

Parameters	1/8-inch diameter mandrel 180 degree bend
Number and Type of Specimens	4 aluminum 2024 series alloy panels per conformal coating alternative
Trials per Specimen	1
Acceptance Criteria	No cracking or crazing

Major or Unique Equipment

1/8-inch diameter mandrel

Data Recording and Calculations

Document appearance and photograph at 10 times magnification

3.2.4. Flame Resistance

Description

The test determines the resistance of a conformal coating film to burning (average burn time, average extent of burn, and self-extinguishing characteristics).

Perform this test in accordance with ASTM D 635-91 (*Standard Test Method for Rate of Burning and/or Extent and Time of Burning of Self-Supporting Plastics in a Horizontal Position*, July 15, 1991), but with the following modifications and additions:

Determine the conformal coating film thickness to ensure that the test specimen has been prepared properly.

Rationale

Conformal coating films must be capable of resisting burning and combustion so as to provide the maximum amount of protection to the circuit card.

Methodology

Table 15. Flame Resistance Methodology

Parameters	• 30 seconds flame exposure • 20 mm blue flame heat source
Number and Type of Specimens	4 type GF laminate strips per conformal coating alternative
Trials per Specimen	1
Acceptance Criteria	Self-extinguishing or non-burning

Major or Unique Equipment

- Bunsen burner or equivalent
- Timer

Data Recording and Calculations

- Time for flame to extinguish
- Distance coating burned
- Average burn time
- Average extent of burn.

3.2.5. Resonance

Description

This test determines the affect of a conformal coating film on the electrical resonance of a circuit.

Perform this test in accordance with the following procedure:

- Measure the resonance of the test specimens at 1 MHz and 50 MHz prior to applying conformal coating material.
- Average the resonance values for each respective frequency.
- Apply conformal coating material to specimens and cure or dry to manufacturer's specifications
- Measure the resonance of the coated test specimen at 1 MHz and 50 MHz.
- Average the resonance values for each respective frequency.
- Immerse the test specimens in distilled water for 24 + 2, -0 hours.
- Remove the test specimens from the water and measure resonance at 1 MHz and 50 MHz within 5 hours.
- Average the resonance values for each respective frequency. Conduct Thermal Shock (3.2.8) with these same specimens.

Rationale

This test is specified by MIL-I-46058C (*Insulating Compound, Electrical (For Coating Printed Wire Assemblies)*, September 1993.)

Immersion in water confirms that the coating will not allow excessive resonance changes in high moisture environments.

Methodology

Table 16. Resonance Methodology

Parameters	1 MHz 50 MHz
Number and Type of Specimens	4 MIL-I-46058C Y coupons per conformal coating alternative
Trials per Specimen	1
Acceptance Criteria	Average percentage change in Q shall not exceed the values specified in the Table 17, Q Resonance Acceptance Criteria, listed below.

Table 17. Q Resonance Acceptance Criteria

Conditioning	**Measurement Frequency (MHz)**	**Maximum Allowable Percentage Change in Q**				
		Acrylic Resin	Epoxy Resin	Silicone Resin	Urethane Resin	Parylene
Before and After Coating	1 50	9 19	8 10	8 12	5 8	9 7
Before and After Immersion (Condition in Distilled Water, D-24/23)	1 50	9 5	12 15	10 12	10 10	11 7

Major or Unique Equipment

Q-meter

Data Recording and Calculations

Resonance readings

3.2.6. Thermal Shock

Description

This test determines the resistance of a conformal coating film to the exposure of high and low temperature extremes.

Perform this test in accordance with the following procedure:

- Equilibrate a temperature chamber to -65 ± 5°C
- Equilibrate another temperature chamber to 125 ± 5°C
- Place the test specimens into a fixture
- Place the fixture into the cold chamber for 30 minutes
- Remove the fixture and place it into the hot chamber for 30 minutes
- Repeat the cold/hot cycle for 50 cycles
- Condition the test specimens at room temperature and 50% ± 5% relative humidity for 24 hours
- Perform the dielectric withstanding voltage test (see JTP Section 3.2.7).

Rationale

MIL-STD-202F, Method 107G (*Test Methods for Electronic and Electrical Component Parts,* March 1984) specifies this test to evaluate conformal coating films.

Methodology

Table 18. Thermal Shock Methodology

Parameters	50 cycles -65°C ± 5°C 125°C ± 5°C
Number and Type of Specimens	4 MIL-I-46058 Y coupons used in 3.2.5.
Trials per Specimen	1
Acceptance Criteria	Smooth, homogeneous, transparent, and unpigmented No bubbles, pinholes, whitish spots, blistering, wrinkling, cracking, or peeling No masking or obliteration of identification markings No discoloration of printed conductors and base materials No corrosion

Major or Unique Equipment

Two temperature chambers capable of -65°C ± 5°C and 125°C ± 5°C, respectively

Data Recording and Calculations

- Document appearance and photograph at 10 times magnification
- Measure current leakage in accordance with the dielectric withstanding voltage test (see JTP Section 3.2.7).

3.2.7. Dielectric Withstanding Voltage

Description

This test determines the dielectric properties of a conformal coating film.

Perform this test in accordance with the following procedure:

- Connect a test specimen to an AC voltage source
- Ramp the test voltage from zero to 1500 V at 500 V_{rms}/second
- Maintain the voltage for 60 seconds
- Measure and record the leakage current.

Rationale

MIL-STD 202F, Method 301 (*Test Methods for Electronic and Electrical Component Parts, Dielectric Withstanding Voltage*, February 1956) specifies this test to evaluate conformal coating films.

Methodology

Table 19. Dielectric Withstanding Voltage Methodology

Parameters	0 V to 1500 V AC at 500 V rms/second ramp
Number and Type of Specimens	4 MIL-I-46058 Y coupons used in 3.2.5 and 3.2.6.
Trials per Specimen	1
Acceptance Criteria	≤ 10 microamperes

Major or Unique Equipment

- 1500 V AC power supply
- Ammeter

Data Recording and Calculations

Leakage current

3.2.8. Insulation Resistance

Description

This test determines the resistance to an impressed direct voltage of a conformal coating film.

Perform this test in accordance with the following procedure:

- Apply 500 V DC to a test specimen
- After one minute, measure the insulation resistance using a MΩ bridge.

Rationale

MIL-STD 202, Method 302 (*Test Methods for Electronic and Electrical Component Parts, Insulation Resistance*, February 6, 1956) specifies this test to evaluate conformal coating films. Impressed direct voltage tends to produce a leakage current through or on the surface of a conformal coating film.

Methodology

Table 20. Insulation Resistance Methodology

Parameters	500 V DC
Number and Type of Specimens	4 MIL-I-46058C Y coupons per conformal coating alternative
Trials per Specimen	1
Acceptance Criteria	Each $\geq 1.5 \times 10^{12}$ ohms under ambient conditions. Average $\geq 2.5 \times 10^{12}$ ohms under ambient conditions.

Major or Unique Equipment

MΩ bridge

Data Recording and Calculations

Calculate average insulation resistance

3.2.9. Moisture Resistance

Description

This test determines the resistance of a conformal coating film to accelerated effects of high humidity and heat conditions.

Perform this test in accordance with the procedure listed below.

- Place the test specimens into a dry oven and condition them at 50°C ± 5°C for 24 hours.
- Remove the specimens from the oven. Condition them at ambient temperature and humidity for two and one-half hours.
- Use a test apparatus that enables the specimens to be subjected to a voltage while in the chamber. This apparatus is similar to a terminal strip, and must be located outside the chamber. It must be able to isolate each individual specimen to read resistance, and be able to apply a voltage to either a single specimen or all specimens at once.
- Load the specimens in the chamber upon a non-conductive surface that will not allow condensation pools to develop, and connect them to the terminal strip. Connect MΩ bridge to terminal strip. Ensure continuity between the specimens and the terminal strip, and that no coupons are touching each other or the chamber walls.
- Equilibrate the chamber to 25 ± 5°C and 90 to 100 percent relative humidity. Using the MΩ bridge, apply the 100 V DC load to all coupons via the terminal strip.
- Linearly ramp the temperature within the chamber to 65°C ± 5°C over a period of two and one-half hours while maintaining the relative humidity at 90% to 100%. Maintain the temperature at 65°C ± 5°C and the relative humidity at 90% to 100% for three hours.
- Linearly ramp the temperature to 25°C ± 5°C over a period of two and one-half hours while maintaining the relative

humidity at 90% to 100%. Maintain the temperature at 25°C ± 5°C and the relative humidity at 90% to 100% for three hours.

- Repeat the temperature increase/hold/decrease/hold process for a total of 10 cycles.
- At the completion of the first, fourth, seventh, and tenth cycles, remove the 100 V DC bias. Isolate the specimens from each other electrically with the terminal strip. Using the MΩ bridge, apply 500 V DC and conduct Insulation Resistance Test (Section 3.2.10) for each specimen individually without removing them from the chamber. After the tenth cycle is complete, conduct Insulation Resistance Test (Section 3.2.10) for each specimen at ambient conditions. Conduct Appearance Test (Section 3.2.2) and Dielectric Withstanding Voltage Test (Section 3.2.9) on these same specimens.

Rationale

MIL-STD 202F, Method 106 (*Test Methods for Electronic and Electrical Component Parts, Moisture Resistance*, June 1990) specifies this test to evaluate conformal coatings. This test simulates the high humidity and heat of tropical environments. The absorption of moisture under these conditions may result in corrosion and subsequent surface insulation resistance failures. High moisture environments will also effect resistance due to the presence of moisture alone, before effects of aging and corrosion occur. The insulation resistance for each coating must be evaluated while the specimen is under moisture exposure. Insulation Resistance Testing the specimens outside of the moisture environment will not accurately reflect performance of the coating.

Methodology

Table 21. Moisture Resistance Methodology

Parameters	• 100V DC • 10 cycles • 25°C to 65°C ± 5°C • 90% to 100% relative humidity
Number and Type of Specimens	4 MIL-I-46058 Y coupons used in 3.2.8.

(Table 21 continued on next page)

Table 21. Moisture Resistance Methodology (Continued)

Trials per Specimen	1
Acceptance Criteria	Smooth, homogeneous, transparent, and unpigmented No bubbles, pinholes, whitish spots, blistering, wrinkling, cracking, or peeling No masking or obliteration of identification markings No discoloration of printed conductors and base materials No corrosion $\leq$ 10 μA current leakage on subsequent Dielectric Withstanding Voltage tests Each acrylic resin, silicone resin, urethane resin, parylene $\geq 5.0 \times 10^9$ Ω while under moisture environment Each epoxy resin $\geq 5.0 \times 10^8$ Ω while under moisture environment Average acrylic resin, silicone resin, urethane resin, parylene $\geq 1.0 \times 10^{10}$ Ω while under moisture environment Average epoxy resin $\geq 1.0 \times 10^9$ Ω while under moisture environment.

Major or Unique Equipment

- Temperature/humidity chamber capable of 25°C to 65°C ± 5°C and 90% to 100% relative humidity ± 4%
- Megohm Bridge
- Test apparatus similar to a terminal block. Apparatus should allow application of a voltage to all specimens simultaneously, and also individually when required.

Data Recording and Calculations

- Appearance
- Dielectric withstanding voltage
- Insulation resistance

3.2.10. Thermal-Humidity Aging

Description

This test determines the ability of a conformal coating film to withstand elevated temperature and humidity-induced failures such as reversion, blistering, peeling, or discoloration.

Perform this test in accordance with the procedure listed below.

- Maintain one test specimen as a control at 25°C and 50% relative humidity.
- Load the remaining specimens into a temperature/humidity chamber and expose them to 85°C ± 1°C and 95% ± 4% relative humidity for 120 days.
- After 28, 56, and 84 days of exposure, remove the specimens from the chamber and condition them at room temperature and 50% relative humidity for two hours. Visually inspect and photograph the specimens under 10 times magnification using both visible and ultraviolet light for signs of softening, chalking, blistering, cracking, tackiness, loss of adhesion, or reversion to a solution state.
- After inspection, return the specimens to the chamber. After 120 days total exposure, remove the specimens from the chamber and condition them at room temperature and 50% relative humidity for seven days. Visually inspect the specimens as specified above. Test the specimens for adhesion (JTP Section 3.2.11).

Rationale

MIL-I-46058C, Paragraph 3.15 (*Insulating Compound, Electrical (For Coating Printed Circuit Card Assemblies)*, September 1993) specifies this test to evaluate conformal coating films.

Methodology

Table 22. Thermal-Humidity Aging Methodology

Parameters	• 120 days • 85°C ± 1°C • 95% ± 4% relative humidity
Number and Type of Specimens	4 MIL-I-46058C Y coupons per conformal coating alternative
Trials per Specimen	1
Acceptance Criteria	No evidence of reversion as indicated by softening, chalking, blistering, cracking, tackiness, loss of adhesion, or liquefaction No loss of legibility and distinguishability of identification markings and color codes used to identify parts Adhesion rating ≥ 4

Major or Unique Equipment

Temperature/humidity chamber capable of maintaining a temperature between 25°C to 100°C and relative humidity between 50% and 100%.

Data Recording and Calculations

- Appearance
- Adhesion rating

Rate the adhesion by assigning an integer from 0 to 5 based on the scale provided in Table 23.

Table 23. Adhesion Rating Scale for Thermal-Humidity AgingTest

Rating	Basis
0	More than 65% of the coating is removed.
1	The coating has flaked in large ribbons along the edges of cuts, and whole lattice squares have detached. The area affected is 35% to 65% of the lattice.
2	The coating has flaked along the edges and on parts of the lattice squares. The area affected is 15% to 35% of the lattice.

(Table 23 continued on next page)

Table 23. Adhesion Rating Scale for Thermal-Humidity Aging Test (Continued)

Rating	Basis
3	Small flakes of the coating are detached along edges and at intersections of cuts. The area affected is 5% to 15% of the lattice.
4	Small flakes of the coating are detached at intersections. Less than 5% of the lattice is affected.
5	The edges of the cuts are smooth. None of the lattice is detached.

3.2.11. Adhesion

Description

This test determines the adhesion of a conformal coating film.

Perform this test in accordance with ASTM D 3359-95a, Method B (*Standard Test Methods for Measuring Adhesion by Tape Test*, December 10 1995). For coating thickness up to and including 2.0 mils, which includes the anticipated conformal coating film thickness, space the required cuts 0.04 inches (1 mm) apart and perform 11 cuts. Make all cuts 0.75 inches (20 mm) long.

Rationale

This test evaluates the adhesion of coatings to substrates both before and after environmental stress.

Methodology

Table 24. Adhesion Methodology

Parameters	Ambient temperature and humidity
Number and Type of Specimens	3 type GF laminate strips per conformal coating alternative
Trials per Specimen	1
Acceptance Criteria	Rating ≥ 4

Major or Unique Equipment

Adhesion test kit

Data Recording and Calculations

- Specific tape used, its manufacturer, and its adhesive strength
- Environmental conditions at time of testing
- Adhesion rating

Rate the adhesion by assigning an integer from 0 to 5 based on the scale provided in Table 25.

Table 25. Adhesion Rating Scale for Adhesion Test

Rating	Basis
0	More than 65% of the coating is removed.
1	The coating has flaked in large ribbons along the edges of cuts, and whole lattice squares have detached. The area affected is 35% to 65% of the lattice.
2	The coating has flaked along the edges and on parts of the lattice squares. The area affected is 15% to 35% of the lattice.
3	Small flakes of the coating are detached along edges and at intersections of cuts. The area affected is 5% to 15% of the lattice.
4	Small flakes of the coating are detached at intersections. Less than 5% of the lattice is affected.
5	The edges of the cuts are smooth. None of the lattice is detached.

3.3. Electrical Performance Tests

Unless otherwise specified, electrical performance tests should be performed on each test specimen prior to and after completing of applicable validation tests. Failure of a test specimen in a specific electrical performance test does not necessarily disqualify a candidate conformal coating material or alternative surface finish for use in an application in which that type of electrical performance is not applicable. (Refer to Appendix B for a more detailed description of the electrical performance tests. Refer to Appendix C for a detailed description of the CCAMTF Automated Test Set (ATS).)

No preferred order exists for performing the tests. The CCAMTF ATS is capable of performing the tests in any sequence.

3.3.1. High Current, Low Voltage (HCLV)

Description

This test determines the resistance in a circuit as a function of voltage.

Perform this test in accordance with the following procedure:

- Place a test specimen in the CCAMTF ATS
- Apply a 5 A direct current using a 100 μs square wave pulse width
- Record the resulting voltage output.

Rationale

Performance of high-current circuits is affected by series resistance. Resistance is most likely to change due to cracking or corrosion of the solder joint that may be related to the soldering process. These conditions decrease the cross-sectional area of the solder joints, thus increasing resistance. Use of high current to test solder-joint resistance makes it easier to detect a change in resistance. A 5 A current has been selected as a value that covers most military applications. A change of resistance is most conveniently determined by measuring the steady state performance of the circuit at a pulse width of 100 μs. This pulse width is long enough for the circuit to achieve steady state before the measurement is taken.

Methodology

Table 26. High Current, Low Voltage (HCLV) Methodology

Parameters	5 A induced current 100 μs pulse width
Acceptance Criteria	$\Delta V < 0.50$ V

Major or Unique Equipment

CCAMTF ATS

Data Recording and Calculations

- HCLV PTH voltage
- HCLV SMT voltage

3.3.2. High Voltage, Low Current (HVLC)

Description

This test determines changes in resistance as a function of current when a high voltage is applied to a circuit.

Perform this test in accordance with the following procedure:

- Place a test specimen in the CCAMTF ATS
- Apply 250 V
- Measure the output current.

Rationale

The insulation resistance between conductors may be reduced by flux residues, surface finish, and conformal coating. The impact of this decrease in resistance could be significant in circuits with a high-voltage gradient across the insulating region. Decreased resistance can be detected by an increase in current when a high voltage is applied to the circuit. A voltage of 250V was selected as the high potential for this test because it represents most military applications. The change in leakage current is determined by measuring the steady-state output of the circuit.

Methodology

Table 27. High Voltage, Low Current Methodology

Parameters	Applied voltage of 250 V
Acceptance Criteria	Output current between 4 to 6 μA

Major or Unique Equipment

CCAMTF ATS

Data Recording and Calculations

- HVLC PTH current
- HVLC SMT current

3.3.3. High Speed Digital (HSD)

Description

This test determines the gate switching speed of an integrated circuit.

Perform this test in accordance with the following procedure:

- Place a test specimen in the CCAMTF ATS
- Apply 5 V
- Measure the propagation delay time.

Rationale

The gate switching speed will be affected by the presence of flux residues, surface finish, conformal coating and environmental conditions.

Methodology

Table 28. High Speed Digital Methodology

Parameters	5 V ± 0.5 V applied DC voltage
Acceptance Criteria	≤ 20% increase in propagation delay time from baseline

Major or Unique Equipment

CCAMTF ATS

Data Recording and Calculations

- HSD PTH propagation delay time
- HSD SMT propagation delay time

3.3.4. High Frequency, Low Pass Filter (LPF)

Description

This test determines surface finish and conformal coating film effects on the performance of high-frequency, LPF printed circuit inductors and transmission lines caused by parasitic resistance and parasitic capacitance. Perform this test in accordance with the following procedure:

- Place a test specimen in the CCAMTF ATS
- Measure the transfer function (T_f):

  T_f (dB) = 20 Log_{10} (V_{out} / V_{in})

Rationale

Changes in surface finish, conformal coating, or flux residues may affect the performance of LPF printed circuit inductors and transmission lines due to parasitic resistance and parasitic capacitance. When a sine wave test signal is passed through an LPF, its amplitude is attenuated as a function of frequency. The relationship between the output and input voltage amplitudes can be expressed as a transfer function. The transfer function, V_{out} / V_{in}, can be measured to determine effects of changes in surface finish, conformal coating, or flux residues.

Methodology

Table 29. High- Frequency (HF) Low Pass Filter (LPF) Methodology

Parameters	Applied frequency between 50 MHz and 1 GHz
Acceptance Criteria	• High-frequency, LPF PTH 50 MHz response in dB: ± 5 dB of the average response of the five HASL PWAs coated with parylene and processed with LR flux at the current test time • High-frequency, LPF PTH frequency response at -3 dB in MHz: ± 50 MHz of the average response of the five HASL PWAs coated with parylene and processed with LR flux at the current test time • High-frequency, LPF PTH frequency response at -40 dB in MHz: ± 50 MHz of the average response of the five HASL PWAs coated with parylene and processed with LR flux at the current test time

(Table 29 continued on next page)

Table 29. High- Frequency (HF) Low Pass Filter (LPF) Methodology (Continued)

	• High-frequency, LPF SMT 50 MHz response in dB: ± 5 dB of the average response of the five HASL PWAs coated with parylene and processed with LR flux at the current test time • High-frequency, LPF SMT frequency response at -3 dB in MHz: ± 50 MHz of the average response of the five HASL PWAs coated with parylene and processed with LR flux at the current test time • High-frequency, LPF SMT frequency response at -40 dB in MHz: ± 50 MHz of the average response of the five HASL PWAs coated with parylene and processed with LR flux at the current test time

Major or Unique Equipment

CCAMTF ATS

Data Recording and Calculations

- HF LPF PTH 50 MHz response in dB
- HF LPF PTH frequency response at -3 dB in MHz
- HF LPF PTH frequency response at -40 dB in MHz
- HF LPF SMT 50 MHz response in dB
- HF LPF SMT frequency response at -3 dB in MHz
- HF LPF SMT frequency response at -40 dB in MHz

3.3.5. High-Frequency (HF) Transmission Line Coupler (TLC)

Description

This test determines surface finish and conformal coating film effects on the performance of high frequency TLCs caused by parasitic resistance and parasitic capacitance.

Perform this test in accordance with the following procedure:

- Place a test specimen in the CCAMTF ATS
- Test the TLC with a sine wave signal
- Connect the three output terminals to 50Ω loads
- Use a source resistance of 50Ω
- Measure the transmission line forward couple signal gain (loss) in dB at frequencies of 50 MHz, 500 MHz and 1 GHz
- Measure the transmission line reverse coupling signal gain (loss) in dB for frequencies from 50 MHz to 1 GHz
- Determine the null gain (dB) and the corresponding frequency (MHz).

Rationale

Surface finish, conformal coating, or flux residues may affect the performance of LPF printed circuit inductors and transmission lines due to parasitic resistance and parasitic capacitance.

Methodology

Table 30. High-Frequency Transmission Line Coupler Methodology

Parameters	Applied frequency between 50 MHz and 1 GHz
Acceptance Criteria	• High-frequency, TLC 50 MHz forward response in dB: ± 5 dB applied on a PWA-to-PWA basis from the current test time to the pre-test • High-frequency, TLC 500 MHz forward response in dB: ± 5 dB applied on a PWA-to-PWA basis from the current test time to the pre-test • High-frequency, TLC 1 GHz forward response in dB: ± 5 dB applied on a PWA-to-PWA basis from the current test time to the pre-test • High-frequency, TLC reverse null frequency response in MHz: ±50 MHz applied on a PWA-to-PWA basis from the current test time to the pre-test

(Table 30 continued on next page)

Table 30. High-Frequency Transmission Line Coupler Methodology (Continued)

	• High-frequency, TLC reverse null response in dB: ± 5 dB applied on a PWA-to-PWA basis from the current test time to the pre-test if the pre-test and current measurements are both greater than –50dB; or ± 10 dB applied on a PWA-to-PWA basis from the current test time to the pre-test if either the pre-test measurement or current measurement are less than –50dB • High-frequency, TLC reverse null frequency in MHz : ± 50 MHz applied on a PWA-to-PWA basis from the current test time to the pre-test

Major or Unique Equipment

CCAMTF ATS

Data Recording and Calculations

- HF TLC 50 MHz forward response in dB
- HF TLC 500 MHz forward response in dB
- HF TLC 1 GHz forward response in dB
- HF TLC reverse null frequency response in MHz
- HF TLC reverse null response in dB

3.3.6. Other Networks (ON)

Description

This test determines the current leakage for a typical circuit layout as a function of processing, surface finishing, conformal coating, and environmental conditions. Leakage current will be expressed as a function of surface insulation resistance.

Perform this test in accordance with the following procedure:

- Attach a test specimen to the CCAMTF ATS
- Apply 100 V
- Measure the resultant leakage current and report in ohms.

Rationale

The pin-grid array, gull wing, and 10-mil pads (see Appendix B) allow leakage currents to be measured. The presence of residues combined with the environmental exposure may increase current leakage.

Methodology

Table 31. Other Networks Methodology

Parameters	100 V
Acceptance Criteria	$\geq 5 \times 10^7\ \Omega$

Major or Unique Equipment

CCAMTF ATS

Data Recording and Calculations

- 10-mil spaced pads current leakage
- PGA-A current leakage
- PGA-B current leakage
- Gull wing current leakage

3.3.7. Stranded Wires (SW)

Description

This test determines the resistance in an insulated 22-gauge stranded wire circuit as a function of voltage.

Perform this test in accordance with the following procedure:

- Solder one wire to two turret terminals, and the second wire to two plated through-holes on a test specimen
- Place the specimen in the CCAMTF ATS
- Apply a 5 A current at a 100 μs pulse width to the SW portion of the test specimen
- Record the resulting voltage output.

Rationale

Performance of high-current circuits is affected by series resistance. Resistance is most likely to change due to cracking or corrosion of the conductor that may be related to the soldering process. These conditions decrease the cross-sectional area of the solder joints, thus increasing resistance. Use of high current to test solder joint resistance makes it easier to detect a change in resistance. A 5 A current has been selected as a value that covers most military applications. A change of resistance is

most conveniently determined by measuring the steady state performance of the circuit at a pulse width of 100 μs. This pulse width is long enough for the circuit to achieve a steady state before the measurement is taken.

Methodology

Table 32. Stranded Wires Methodology

Parameters	5 A induced current 100 μs pulse width
Acceptance Criteria	$\Delta V < 0.356$ V

Major or Unique Equipment

CCAMTF ATS

Data Recording and Calculations

- Stranded wire 1 voltage
- Stranded wire 2 voltage.

3.4. Environmental Exposure Tests

3.4.1. Environmental 85°C/85% Relative Humidity (RH)

Description

This test determines a test specimen's performance after exposure to thermal-humidity aging conditions.

Perform this test in accordance with the procedure listed below.

- Test the HCLV, HVLC, HSD, HF, ON, and SW electrical performance of five PWAs of each alternative surface finish/conformal coating combination prior to exposure, and record the results.
- Place the PWAs into a test rack in random order and place the test rack into a temperature/humidity chamber. Initialize the chamber at 25°C and 50% relative humidity. Equilibrate the chamber under these conditions for two hours. Increase the temperature to 85°C over thirty minutes. Maintain that temperature for two hours. Increase the relative humidity to 85% over thirty minutes. After two hours at 85°C and 85% relative humidity, apply bias voltages as specified in Table 31.

- After 168 hours (one week), discontinue the bias voltage. Decrease the relative humidity to 50% over thirty minutes. At 50% relative humidity, decrease the temperature to 25°C over thirty minutes. Equilibrate the chamber under these conditions (25°C, 50% relative humidity) for two hours. Remove and test the PWAs (HCLV, HVLC, HSD, HF, ON, and SW electrical performance).
- Reinstall the PWAs and repeat the temperature, relative humidity, and voltage cycles above for two additional one week intervals. Test the HCLV, HVLC, HSD, HF, ON, and SW electrical performance of the PWAs at the end of each subsequent week.

Rationale

MIL-PRF-38535D (*General Specification for Integrated Circuits (Microcircuits) Manufacturing*, April 15, 1996) specifies this test to evaluate circuits. IPC-TM-650 Method 2.6.3.3 Rev. A (*Surface Insulation Resistance, Fluxes*, January 1995) also specifies this test.

Methodology

Table 33. Environmental 85°C/85% Relative Humidity Methodology

Parameters	• 5 V ± 0.5 V DC bias applied continually to the high speed digital (HSD) section only • 250 V bias applied one hour per day to high voltage low current (HVLC) section only • 100 V bias applied continuously to the pin-grid array, gull wing & 10-mil pads section only • No bias applied to high current low voltage (HCLV), high frequency (HF), and stranded wire (SW) sections • 85°C • 85% relative humidity • 3 week exposure
Number and Type of Specimens	5 PWAs per alternative surface finish/conformal coating combination
Trials per Specimen	1
Acceptance Criteria	Refer to Data Recording & Calculations

Major or Unique Equipment

- Temperature/humidity chamber
- CCAMTF ATS
- Power supply

Data Recording and Calculations

- Attach chart recorder graph from the temperature/humidity chamber.
- Record data and compare to acceptance criteria as specified in JTP sections:

  3.3.1. High Current, Low Voltage (HCLV)
  3.3.2. High Voltage, Low Current (HVLC)
  3.3.3. High Speed Digital (HSD)
  3.3.4. High Frequency Low Pass Filter (LPF)
  3.3.5. High Frequency Transmission Line Coupler (TLC)
  3.3.6. Other Networks (ON)
  3.3.7. Stranded Wire (SW).

- Document appearance per ANSI/J-STD-001, Class 3 (*Requirements for Soldered Electrical and Electronic Assemblies*, October 1996) and photograph at 10 times magnification.

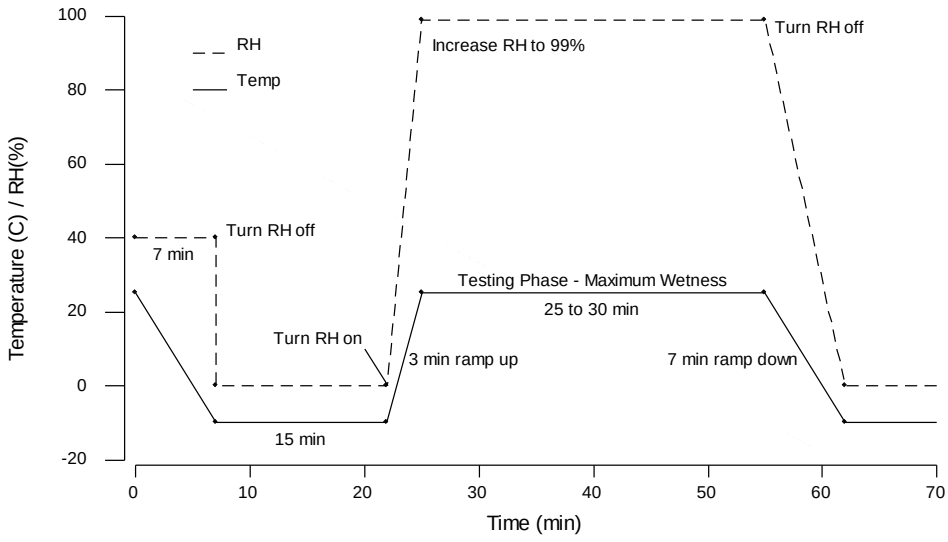
3.4.2. Condensing Atmosphere

Description

This evaluation determines a specimen's performance under condensing moisture conditions.

Perform this test in accordance with the following procedure:

- Test the HCLV, HVLC, HSD, HF, ON, and SW electrical



- Figure 10. Temperature and Humidity Profiles for One Cycle of the Condensing Atmosphere Test

- Perform the temperature and humidity cycle 10 times.
- Perform the HCLV, HVLC, HSD, HF, ON, and SW electrical performance tests during the first, fourth, seventh and tenth cycles. Electrical biases are applied during the non-electrical test cycles. Record the results.

Rationale

MIL-STD-883E Method 1004.7 (*Test Method Standard Microcircuits, Moisture Resistance*, August 17, 1987) specifies this test to evaluate moisture resistance.

Methodology

Table 34. Condensing Atmosphere Methodology

Parameters	• 10 cycles • 5 V ± 0.5 V DC bias applied to the high speed digital (HSD) section only • 250 V bias applied to high voltage, low current (HVLC) section only • 100 V bias applied to the pin-grid array, gull wing & 10-mil pads section only • No bias applied to high current, low voltage (HCLV), high frequency (HF), and stranded wire (SW) sections

(Table 34 continued on next page)

Table 34. Condensing Atmosphere Methodology (Continued)

Number and Type of Specimens	5 PWAs per alternative surface finish/conformal coating combination
Trials per Specimen	1
Acceptance Criteria	See Data Recording & Calculations

Major or Unique Equipment

- Temperature/humidity chamber
- CCAMTF ATS
- Fixture
- Power Supply

Data Recording and Calculations

- Attach chart recorder graph from the temperature/humidity chamber.
- Record data and compare to acceptance criteria as specified in JTP sections:
  3.3.1. High Current, Low Voltage (HCLV)
  3.3.2. High Voltage, Low Current (HVLC)
  3.3.3. High Speed Digital (HSD)
  3.3.4. High Frequency Low Pass Filter (LPF)
  3.3.5. High Frequency Transmission Line Coupler (TLC)
  3.3.6. Other Networks (ON)
  3.3.7. Stranded Wire (SW).

- Document appearance per ANSI/J-STD-001, Class 3 (*Requirements for Soldered Electrical and Electronic Assemblies*, October 1996) and photograph at 10 times magnification.

3.4.3. Fluid Exposure - Diesel Fuel

Description

This test determines a test specimen's resistance to degradation from contact with diesel fuel.

Perform this test in accordance with the following procedure:

- Test the HCLV, HVLC, HSD, HF, ON, and SW electrical performance of five PWAs of each alternative surface finish/conformal coating combination prior to exposure and record the results.
- Mask all connectors. Equilibrate the diesel fuel at room temperature. Dip the specimen into the fluid and soak for 10 minutes. Record the fluid temperature, ambient temperature, and relative humidity.
- Remove the specimen from the fluid and allow it to drip dry for 30 minutes. Remove any remaining fluid by wiping the specimen with a lint free cloth. Repeat dipping for specified time (into fresh fluid), soaking, drying, and wiping. Remove masking and air dry for 24 hours minimum.
- Measure and record the HCLV, HVLC, HSD, HF, ON, and SW electrical performance for each PWA.

Rationale

This test is based on the requirements of SAE J1211 (*Recommended Environmental Practices for Electronic Equipment Design*, November 1978). Diesel fuel is a typical fluid encountered in military applications.

Methodology

Table 35. Fluid Exposure - Diesel Fuel Methodology

Parameters	• 10 minute soak • 2 dips
Number and Type of Specimens	5 PWAs per alternative surface finish/conformal coating combination
Trials per Specimen	1
Acceptance Criteria	Refer to Data Recording & Calculations

Major or Unique Equipment

- CCAMTF ATS
- Type 2 diesel fuel
- Solvent-resistant masking

Data Recording and Calculations

- Record data and compare to acceptance criteria as specified in JTP sections:

  3.3.1. High Current, Low Voltage (HCLV)
  3.3.2. High Voltage, Low Current (HVLC)
  3.3.3. High Speed Digital (HSD)
  3.3.4. High Frequency Low Pass Filter (LPF)
  3.3.5. High Frequency Transmission Line Coupler (TLC)
  3.3.6. Other Networks (ON)
  3.3.7. Stranded Wire (SW).

- Document appearance per ANSI/J-STD-001, Class 3 (*Requirements for Soldered Electrical and Electronic Assemblies*, October 1996) and photograph at 10 times magnification.

3.4.4. Fluid Exposure - Hydraulic Fluid

Description

This evaluation determines a specimen's resistance to degradation from contact with hydraulic fluid.

Perform this test in accordance with the following procedure:

- Test the HCLV, HVLC, HSD, HF, ON, and SW electrical performance of five PWAs of each alternative surface finish/conformal coating combination prior to exposure and record the results.
- Mask all connectors. Equilibrate the hydraulic fluid at room temperature. Dip the specimen into the fluid and soak for 10 minutes. Record the fluid temperature, ambient temperature, and relative humidity.
- Remove the specimen from the fluid and allow it to drip dry for 30 minutes. Remove any remaining fluid by wiping the specimen with a lint free cloth. Repeat dipping for specified time (into fresh fluid), soaking, drying, and wiping. Remove the masking.
- Measure and record the HCLV, HVLC, HSD, HF, ON, and SW electrical performance for each PWA.

Rationale

This test is based on the requirements of SAE J1211 (*Recommended Environmental Practices for Electronic Equipment Design*, November 1978). Hydraulic fluid is a typical fluid encountered in military applications.

Methodology

Table 36. Fluid Exposure - Hydraulic Fluid Methodology

Parameters	• 10 minute soak • 2 dips
Number and Type of Specimens	5 PWAs per alternative surface finish/conformal coating combination
Trials per Specimens	1
Acceptance Criteria	Refer to Data Recording & Calculations

Major or Unique Equipment

- CCAMTF ATS
- MIL-H-87257 Hydraulic Fluid
- Solvent-resistant masking

Data Recording and Calculations

- Record data and compare to acceptance criteria as specified in JTP sections:

  3.3.1. High Current, Low Voltage (HCLV)
  3.3.2. High Voltage, Low Current (HVLC)
  3.3.3. High Speed Digital (HSD)
  3.3.4. High Frequency Low Pass Filter (LPF)
  3.3.5. High Frequency Transmission Line Coupler (TLC)
  3.3.6. Other Networks (ON)
  3.3.7. Stranded Wire (SW).

- Document appearance per ANSI/J-STD-001, Class 3 (*Requirements for Soldered Electrical and Electronic Assemblies*, October 1996) and photograph at 10 times magnification.

3.4.5. Branch Water Test (Condensed Moisture Test)

Description

This test determines the moisture condensation protection provided by a conformal coating film.

Perform this test in accordance with the following procedure:

- Obtain a sample of tap water and measure its conductance using a conductivity meter. If the conductance is not 1000 ± 400 micromho ("standard conductance"), adjust the conductance by diluting it with deionized water to reduce conductance, or by adding a few drops of sodium chloride (NaCl) solution to increase conductance.
- Prepare one liter of spray solution by partially filling a 1 liter flask with standard conductance tap water and adding 1.0 ml concentrated liquid dish detergent. Dilute to volume with additional standard conductance tap water and mix well. Fill a hand pump sprayer (i.e., glass cleaner type spray container) to approximately 75% of its capacity. Pump the sprayer until a steady amount of liquid is delivered with each pump stroke. Adjust the pump spray nozzle to deliver a fine spray mist of 6 grams with three pump strokes. (The mass of water delivered is determined by measuring the mass of the sprayer both before and after spraying.) Mark this setting on the nozzle for easy reference. Repeat this procedure for a second hand pump using deionized water instead of standard conductance solution.
- Test and record the HCLV, HVLC, HSD, HF, ON, and SW electrical performance of the PWA.
- Place the PWA in the vertical position in the CCAMTF ATS. Spray the detergent solution uniformly over both sides of the PWA until a continuous film of solution is visible over the entire PWA. Allow the solution to penetrate around the components and run downward for 3 ± 0.5 minutes. Then test and record the HCLV, HVLC, HSD, HF, ON, and SW electrical performance of the PWA.
- Spray the PWA with approximately 20 ml deionized water to remove the detergent solution. Remove the PWA from the CCAMTF ATS and dry it, using any drying mechanism that will not contaminate the PWA. Replace the PWA in the CCAMTF ATS.
- Test and record the HCLV, HVLC, HSD, HF, ON, and SW electrical performance of the PWA.

- Place the PWA mounted in the horizontal position in the CCAMTF ATS with the backside up. Wet only the side facing up (backside). Allow the solution to penetrate around the components for 3 ± 0.5 minutes. Then test and record the HCLV, HVLC, HSD, HF, ON, and SW electrical performance of the PWA.
- Spray the PWA with approximately 20 ml deionized water to remove the detergent solution. Remove the PWA from the CCAMTF ATS and dry it, using any drying mechanism that will not contaminate the PWA. Replace the PWA in the CCAMTF ATS.
- Test and record the HCLV, HVLC, HSD, HF, ON, and SW electrical performance of the PWA.
- Place the PWA mounted in the horizontal position in the CCAMTF ATS with the component side up. Wet only the side facing up (component side). Allow the solution to penetrate around the components for 3 ± 0.5 minutes. Then test and record the HCLV, HVLC, HSD, HF, ON, and SW electrical performance of the PWA.

Rationale

This test is based on the requirements of MIL-E-5400T (*General Specification for Aerospace Electronic Equipment*, August 14, 1992) and MIL-STD-810. The surfactant is added as a small percentage by volume to lower the surface tension of the solution and achieve a continuous aqueous film across the entire surface of the PWA.

Methodology

Table 37. Branch Water Test (Condensed Moisture Test) Methodology

Parameters	• Ambient temperature • 3 ± 0.5 minute moisture exposure • Test in vertical position, horizontal position with backside facing up, and horizontal position with component side facing up
Number and Type of Specimens	5 PWAs per alternative surface finish/conformal coating combination
Trials per Specimens	3
Acceptance Criteria	• Refer to Data Recording & Calculations • Specimens must pass the test in each of the three specified positions

Major or Unique Equipment

Two hand-pump liquid sprayers with adjustable nozzles

Data Recording and Calculations

- Record data and compare to acceptance criteria as specified in JTP sections:

  3.3.1. High Current, Low Voltage (HCLV)
  3.3.2. High Voltage, Low Current (HVLC)
  3.3.3. High Speed Digital (HSD)
  3.3.4. High Frequency Low Pass Filter (LPF)
  3.3.5. High Frequency Transmission Line Coupler (TLC)
  3.3.6. Other Networks (ON)
  3.3.7. Stranded Wire (SW).

3.4.6. Accelerated Life Test

Description

This test determines the long-term performance of a solder joint connection.

Perform this test in accordance with the following procedure:

- Test the HCLV, HVLC, HSD, HF, ON, and SW electrical performance of five PWAs of each alternative surface finish/conformal coating combination.
- Place the specimens into a temperature chamber. Decrease the temperature of the chamber to -55°C at a rate of 15 ± 2°C/minute. When the temperature of the PWAs (as measured on the PWAs) reaches -40°C, immediately begin increasing the temperature to 95°C at 15 ± 2°C/minute. Repeat the temperature cycle for 1800 cycles.
- At the completion of the 1800th cycle, remove all PWAs and test the HCLV, HVLC, HSD, HF, ON, and SW electrical performance of the PWAs. Sequentially perform the vibration test (JTP Section 3.5.3), the mechanical shock test (JTP Section 3.5.4), and the branch water test (JTP Section 3.4.5) on all PWAs.

Rationale

This test is based on identified needs of the defense system programs. The background of this test was taken from Engelmair's paper (*The Use Environments of Electronic Assemblies and Their Impact on Surface Mount Solder Attachment Reliability*, January 1990).

The test is designed such that eight years of actual operation is simulated by 1800 cycles.

Methodology

Table 38. Accelerated Life Test Methodology

Parameters	• 1800 cycles • Minimum temperature -55°C • Temperature ramp rate 15 ± 2°C/minute • Maximum temperature 95°C
Number and Type of Specimens	5 PWAs per alternative surface finish/conformal coating combination
Trials per Specimen	1
Acceptance Criteria	Refer to Data Recording & Calculations

Major or Unique Equipment

- Temperature chamber with temperature ramp capability
- Temperature chamber temperature chart recorder graph
- CCAMTF ATS

Data Recording and Calculations

- Attach chart recorder graph from the temperature chamber.
- Record data and compare to acceptance criteria as specified in JTP sections:

  3.3.1. High Current, Low Voltage (HCLV)
  3.3.2. High Voltage, Low Current (HVLC)
  3.3.3. High Speed Digital (HSD)
  3.3.4. High Frequency Low Pass Filter (LPF)
  3.3.5. High Frequency Transmission Line Coupler (TLC)
  3.3.6. Other Networks (ON)
  3.3.7. Stranded Wire (SW).

- Document appearance and photograph at 10 times magnification.

3.4.7. Sulfur Dioxide/Salt Fog Resistance

Description

This test determines the resistance of a conformal coating film to accelerated, deleterious effects of exposure to a sulfur dioxide/salt fog.

Perform this test in accordance with ASTM G 85-85 (*Standard Practice for Modified Salt Spray (Fog) Testing*, March 1990), but with the modifications and additions listed below.

- Set the fog chamber temperature to 123°F ± 3°F. Set the bubble tower temperature to 138°F ± 2°F. Prepare a salt solution using one part by volume of ASTM D 1141-95 *(Standard Specification for Substitute Ocean Water*, February 2, 1990) solution in 10 parts distilled water.
- Generate the fog discontinuously; each cycle should consist of five hours with fog generation, and one hour without fog generation.
- Start the sulfur dioxide flow 15 minutes prior to cessation of the salt fog generation, and continue it for 15 minutes into the nongeneration period during each cycle, for a total of 30 minutes of sulfur dioxide exposure during each cycle.
- Place the MIL-I-46058C Y-Coupons into the salt fog chamber.
- Perform the above salt fog exposure for 56 cycles (336 hours).
- At the completion of the 56th cycle, remove all coupons and perform the dielectric withstanding voltage (JTP Section 3.2.7), and insulation resistance (JTP Section 3.2.8) tests.
- Test the HCLV, HVLC, HSD, HF, ON, and SW electrical performance of five PWAs of each alternative surface finish/conformal coating combination which passed the MIL-I-46058C Y-Coupon test.
- Place the PWAs for the alternative surface finish/conformal coating combinations which passed the MIL-I-46058C Y-Coupon test into the salt fog chamber.
- Perform the above salt fog exposure for 56 cycles (336 hours).
- At the completion of the 56th cycle, remove all PWAs and test the HCLV, HVLC, HSD, HF, ON, and SW electrical performance of the PWAs.

Rationale

This test simulates the environmental conditions typically experienced by a defense system situated on an aircraft carrier or on shore locations with considerable air pollution.

Methodology

Table 39. Sulfur Dioxide/Salt Fog Resistance Methodology

Parameters	• Fog chamber temperature: 123°F ± 3°F • Bubble tower temperature: 138°F ± 2°F • 5 hour salt fog generation/1 hour non-fog generation/30 minutes sulfur dioxide exposure per cycle • 56 cycles
Number and Type of Specimens	• 1st run: 4 MIL-I-46058C Y-Coupons per alternative surface finish/conformal coating combination • 2nd run: Alternative surface finish/conformal coating combinations applied to MIL-I-46058C Y-Coupons and meeting the acceptance criteria during the 1st run will be subsequently tested using 5 PWAs per successful alternative surface finish/conformal coating combination
Trials per Specimens	1
Acceptance Criteria	• No corrosion, bubbles, pinholes, blistering, wrinkling, cracking, peeling, masking or obliteration of identification markings, discoloration of printed conductors and base materials • For the MIL-I-46058C Y-Coupon: – Dielectric withstanding voltage < 10 μA – Each acrylic resin, silicone resin, urethane resin and parylene ≥ 5 X 10^9 Ω – Each epoxy resin ≥ 5 X 10^8 Ω – Average acrylic resin, silicone resin, urethane resin and parylene ≥ 1 X 10^{10} Ω – Average epoxy resin ≥ 1 X 10^9 Ω • For the PWA, refer to Data Recording & Calculations

Major or Unique Equipment

Salt fog chamber

Data Recording and Calculations

- Appearance
- For the MIL-I-46058C Y-Coupon:
  - Dielectric withstanding voltage
  - Insulation resistance
  - Average insulation resistance
- For the PWA, record data and compare to acceptance criteria as specified in JTP sections:

  3.3.1. High Current, Low Voltage (HCLV)
  3.3.2. High Voltage, Low Current (HVLC)
  3.3.3. High Speed Digital (HSD)
  3.3.4. High Frequency Low Pass Filter (LPF)
  3.3.5. High Frequency Transmission Line Coupler (TLC)
  3.3.6. Other Networks (ON)
  3.3.7. Stranded Wire (SW)

3.5. Physical Reliability Evaluations

3.5.1. Thermal Shock

Description

This evaluation determines the effect of instantaneous changes between low and high temperature on a specimen.

Perform this test in accordance with the following procedure:

- Test the HCLV, HVLC, HSD, HF, ON, and SW electrical performance of five PWAs of each alternative surface finish/conformal coating combination prior to performing this evaluation and record the results.
- Equilibrate a temperature chamber to -55°C ± 5°C. Equilibrate another temperature chamber to 125°C ± 5°C. Place the test specimens into a fixture. Place the fixture into the colder chamber for 30 minutes. Remove the fixture and place it into the warmer chamber for 30 minutes. Repeat for 100 cycles.
- Test the HCLV, HVLC, HSD, HF, ON, and SW electrical performance of the PWAs and record the results.

- Return the test specimens to the temperature chamber and repeat for 100 cycles.
- Test the HCLV, HVLC, HSD, HF, ON, and SW electrical performance of the PWAs and record the results.

Rationale

This evaluation is based on the requirements of MIL-STD-883E, Method 1010.7 Condition B (*Test Method Standard Microcircuits, Temperature Cycling*, May 1987).

Methodology

Table 40. Thermal Shock Methodology

Parameters	• 200 cycles • Minimum temperature (-55°C) • Maximum temperature (125°C)
Number and Type of Specimens	5 PWAs per alternative surface finish/conformal coating combination
Trials per Specimen	1
Acceptance Criteria	Refer to Data Recording & Calculations

Major or Unique Equipment

- Temperature chamber
- CCAMTF ATS

Data Recording and Calculations

- Attach chart recorder graph from the temperature chamber.
- Record data and compare to acceptance criteria as specified in JTP sections:

  3.3.1. High Current, Low Voltage (HCLV)
  3.3.2. High Voltage, Low Current (HVLC)
  3.3.3. High Speed Digital (HSD)
  3.3.4. High Frequency Low Pass Filter (LPF)
  3.3.5. High Frequency Transmission Line Coupler (TLC)
  3.3.6. Other Networks (ON)
  3.3.7. Stranded Wire (SW).

- Document appearance per ANSI/J-STD-001, Class 3 (*Requirements for Soldered Electrical and Electronic Assemblies*, October 1996) and photograph at 10 times magnification.

3.5.2. Thermal Cycling

Description

This evaluation determines the effect of thermal stresses due to a coefficient of thermal expansion (CTE) mismatch on the electrical performance of a PWA.

Perform this test in accordance with the following procedure:

- Test the HCLV, HVLC, HSD, HF, ON, and SW electrical performance of five PWAs of each alternative surface finish/conformal coating combination prior to performing this evaluation and record the results.
- Place the specimens into a temperature chamber. Lower the temperature to -55°C at ≤ 5°C/minute. Equilibrate the chamber at -55°C for 30 minutes. Increase the temperature at ≤ 5°C/minute to 100°C.
- After 250 cycles, test the HCLV, HVLC, HSD, HF, ON, and SW electrical performance of the PWAs and record the results.
- Return the specimens to the temperature chamber and repeat the thermal cycling. After 250 cycles, test the HCLV, HVLC, HSD, HF, ON, and SW electrical performance of the PWAs and record the results.

Rationale

This evaluation is based on the requirements of MIL-STD-781D (*Reliability Testing for Engineering Development, Qualification, and Production*, October 1986). Thermal cycling evaluations are commonly used for environmental stress screening for infant mortality and qualification testing of PWAs.

Methodology

Table 41. Thermal Cycling Methodology

Parameters	• 500 cycles • Minimum temperature (-55°C) • Temperature ramp rate ≤ 5°C/minute • Maximum temperature (+100°C)
Number and Type of Specimens	5 PWAs per alternative surface finish/conformal coating combination
Trials per Specimen	1
Acceptance Criteria	Refer to Data Recording & Calculations

Major or Unique Equipment

- Temperature chamber with temperature ramp capability
- Temperature chamber temperature chart recorder graph
- CCAMTF ATS

Data Recording and Calculations

- Attach chart recorder graph from the temperature chamber.
- Record data and compare to acceptance criteria as specified in JTP sections:

  3.3.1. High Current, Low Voltage (HCLV)
  3.3.2. High Voltage, Low Current (HVLC)
  3.3.3. High Speed Digital (HSD)
  3.3.4. High Frequency Low Pass Filter (LPF)
  3.3.5. High Frequency Transmission Line Coupler (TLC)
  3.3.6. Other Networks (ON)
  3.3.7. Stranded Wire (SW).

- Document appearance per ANSI/J-STD-001, Class 3 (*Requirements for Soldered Electrical and Electronic Assemblies*, October 1996) and photograph at 10times magnification.

3.5.3. Vibration

Description

This evaluation determines the effect of vibration on a specimen.

Perform this test in accordance with the following procedure:

- Test the HCLV, HVLC, HSD, HF, ON, and SW electrical performance of five PWAs of each alternative surface finish/conformal coating combination prior to performing this evaluation and record the results.
- Test using a random vibration on 3 axis, 5 Hz - 2000 Hz, 2 hours per axis, and 8 g_{rms} to 10 g_{rms} loading on the PWAs.
- Test the HCLV, HVLC, HSD, HF, ON, and SW electrical performance of five PWAs and record the results.

Rationale

This evaluation is based on the requirements of MIL-STD-810E, Method 514.4 (*Test Method Standard for Environmental Engineering Consideration and Laboratory Tests, Vibrational*, July 1989). Vibration testing is performed to determine the equipment resistance to vibrational stresses expected during its shipment and use. Vibration can cause wire chafing, loosening of fasteners, intermittent electrical contacts, touching and shorting of electrical parts, seal deformation, component fatigue, optical misalignment, cracking, and rupturing.

Methodology

Table 42. Vibration Methodology

Parameters	• Frequency: 5 Hz to 2000 Hz along each axis • Gravitational force: 8 g_{rms} to 10 g_{rms} • 2 hours per axis
Number and Type of Specimens	5 PWAs per alternative surface finish/conformal coating combination
Trials per Specimen	1
Acceptance Criteria	Refer to Data Recording & Calculations

Major or Unique Equipment

- Vibration table
- CCAMTF ATS

Data Recording and Calculations

- Record data and compare to acceptance criteria as specified in JTP sections:

  3.3.1. High Current, Low Voltage (HCLV)
  3.3.2. High Voltage, Low Current (HVLC)

3.3.3. High Speed Digital (HSD)
3.3.4. High Frequency Low Pass Filter (LPF)
3.3.5. High Frequency Transmission Line Coupler (TLC)
3.3.6. Other Networks (ON)
3.3.7. Stranded Wire (SW).

- Document appearance per ANSI/J-STD-001, Class 3 (*Requirements for Soldered Electrical and Electronic Assemblies,* October 1996) and photograph at 10 times magnification.

3.5.4. Mechanical Shock

Description

This evaluation determines a specimen's resistance to impact.

Perform this test in accordance with the following procedure:

- Test the HCLV, HVLC, HSD, HF, ON, and SW electrical performance of five PWAs of each alternative surface finish/conformal coating combination prior to performing this evaluation and record the results.
- Mount a PWA in a rectangular fixture. (The fixture should be designed to accommodate the PWA, but actual specifications are left to the discretion of personnel performing the testing.) From a height of 1 meter, drop the PWA onto a concrete surface as follows:
  - Five times on each face of the PWA (10 drops total)
  - Five times on each of the three nonconnector edges of the PWA (15 drops total).
- Test the HCLV, HVLC, HSD, HF, ON, and SW electrical performance of the PWA and record the results.

Rationale

This evaluation is based on the requirements of MIL-STD-810E Method 516.4. (*Test Method Standard for Environmental Engineering Consideration and Laboratory Tests, Shock*, July 1989). Mechanical shock evaluations are commonly used to ensure solder joint strength. This test will determine whether the PWA has maintained sufficient solder joint strength.

Methodology

Table 43. Mechanical Shock Methodology

Parameters	• 1 meter free fall • Concrete surface • 25 drops
Number and Type of Specimens	5 PWAs per alternative surface finish/conformal coating combination
Trials per Specimens	1
Acceptance Criteria	Refer to Data Recording & Calculations

Major or Unique Equipment

- Concrete surface
- CCAMTF ATS
- Rectangular mounting fixture

Data Recording and Calculations

- Record data and compare to acceptance criteria as specified in JTP sections:

  3.3.1. High Current, Low Voltage (HCLV)
  3.3.2. High Voltage, Low Current (HVLC)
  3.3.3. High Speed Digital (HSD)
  3.3.4. High Frequency Low Pass Filter (LPF)
  3.3.5. High Frequency Transmission Line Coupler (TLC)
  3.3.6. Other Networks (ON)
  3.3.7. Stranded Wire (SW).

- Document appearance per ANSI/J-STD-001, Class 3 (*Requirements for Soldered Electrical and Electronic Assemblies*, October 1996) and photograph at 10 times magnification.

4. QUALITY CONTROL TESTS

Quality control testing will be performed on certain test specimens subsequent to validation testing to ensure that (1) the surface finishes have been properly prepared prior to conformal coating, and (2) the conformal coating material was properly applied. Quality control tests are not used to validate the performance of alternative surface finishes and conformal coating films; rather, acceptance criteria are used solely to determine whether a test specimen has been prepared properly. Table 44 summarizes the quality control tests.

Table 44. Quality Control Tests

Quality Control Test Description	JTP Section	Reference	Acceptance Criteria
Coating Adhesion	4.1.1	ATSM D 3359	Adhesion rating ≥ 4
Surface Insulation Resistance	4.1.2	IPC-TM-650 Method 2.6.3.3	$\geq 10^8\ \Omega$

4.1. Quality Control Tests

4.1.1. Coating Adhesion

Description

This test assesses the adhesion of conformal coating films to test specimens.

Perform this test in accordance with ASTM D 3359-95a, Method B (*Standard Test Methods for Measuring Adhesion by Tape Test,* December 1995).

Rationale

This test will be used to document the effect of various environmental stress tests and surface finishes on the adhesion characteristics of parylene, urethane, and silicone conformal coatings. Results of the coating adhesion test will be used to correlate coating adhesion to circuit performance.

Methodology

Table 45. Coating Adhesion Methodology

Parameters	Room temperature
Number and Type of Specimens	• 1 PWA each of parylene, urethane, and silicone conformal coating prior to environmental exposures • 5 PWAs each of parylene, urethane, and silicone conformal coating previously subjected to the environmental 85°C/85 % RH test (JTP Section 3.4.1) and thermal shock test (Section 3.5.1) • 5 PWAs each of parylene, urethane, and silicone conformal coating previously subjected to the condensing atmosphere test (JTP Section 3.4.2) and thermal cycling test (Section 3.5.2) • 5 PWAs each of parylene, urethane, and silicone conformal coating previously subjected to the fluid exposure – diesel fuel test (JTP Section 3.4.3) and hydraulic fluid test (Section 3.4.4) • 5 PWAs each of parylene, urethane, and silicone conformal coating previously subjected to the accelerated life test (JTP Section 3.4.6), the vibration test (Section 3.5.3), the mechanical shock test (Section 3.5.4), and the branch water test (Section 3.4.5) • 5 PWAs of each parylene, urethane, and silicone conformal coating, that were selected for salt spray exposure based on "Y" coupon salt fog results, previously subjected to branch water testing (JTP Section 3.4.5) and salt fog testing (Section 3.4.7) • 96 modified parylene coated IPC-B-24 boards previously subjected to the surface insulation resistance test (JTP Section 3.1.1)
Trials per Specimen	1
Acceptance Criteria	Rating ≥ 4

Major or Unique Equipment

Adhesion test kit

Data Recording and Calculations

- Specific tape used, its manufacturer, and its adhesive strength
- Environmental conditions at time of testing
- Adhesion rating

Rate the adhesion by assigning an integer from 0 to 5 based on the scale provided in Table 46 below.

Table 46. Adhesion Rating Schedule for Adhesion Test

Rating	Basis
0	More than 65% of the coating is removed.
1	The coating has flaked in large ribbons along the edges of cuts and whole lattice squares have detached. The area affected is 35% to 65% of the lattice.
2	The coating has flaked along the edges and on parts of the lattice squares. The area affected is 15% to 35% of the lattice.
3	Small flakes of the coating are detached along edges and at intersections of cuts. The area affected is 5% to 15% of the lattice.
4	Small flakes of the coating are detached at intersections. Less than 5% of the lattice is affected.
5	The edges of the cuts are smooth. None of the lattice is detached.

4.1.2. Surface Insulation Resistance (SIR)

Description

This test determines the surface insulation resistance of a test specimen.

Perform this test in accordance with the following procedure:

- Apply a 50 V bias to a test specimen
- Expose the specimen to an 85°C/85% relative humidity environment for 168 hours

- Use a staggered temperature ramp to prevent condensation on the boards
- Perform SIR measurements after 24, 96, and 168 hours of exposure, and 2 and 24 hours after being removed from exposure.

Rationale

Performing SIR testing compares the performance of parylene conformal coatings with and without the use of primer for the alternative surface finishes and assembly processing conditions under study.

SIR testing is an accelerated aging test. The intent is to accelerate electrochemical failure mechanisms in a fairly short amount of time, which would occur in field service. Failure mechanisms include electrolytic corrosion, electrical leakage, and metal migration (dendritic growth).

This evaluation is based on the requirements of IPC-TM-650, Method 2.6.3.3 (*Institute for Interconnecting and Packaging Electronic Circuits Test Methods Manual, Surface Insulation Resistance, Fluxes, Rev. A*, January, 1995).

Methodology

Table 47. Surface Insulation Resistance Methodology

Parameters	• 50 V applied bias (to increase degradation rate) • 100 V testing voltage • 85°C • 85% relative humidity • 168 hours
Number and Type of Specimens	28 modified IPC-B-24 boards per alternative surface finish/conformal coating combination
Trials per Specimen	1
Acceptance Criteria	$\geq 10^8\ \Omega$

Major or Unique Equipment

- Temperature/Humidity chamber
- 50 V DC bias source

Data Recording and Calculations

- Record SIR measurements at the following time intervals:
  - 0 hours
  - 24 hours
  - 96 hours
  - 168 hours
  - 2 hours post
  - 24 hours post.

- Document appearance and photograph at 10 times magnification.

5. REFERENCE DOCUMENTS

Table 48 summarizes the documents referenced in this JTP.

Table 48. Reference Documents

Reference Document	Title	Date	Applicable Section(s) of Reference Document	JTP Topic	JTP Section
ANSI/J-STD-001	Requirements for Soldered Electrical and Electronic Assemblies	Oct 96	All	Environmental 85°C/85% Relative Humidity	3.4.1
				Condensing Atmosphere	3.4.2
				Fluid Exposure - Diesel Fuel	3.4.3
				Fluid Exposure - Hydraulic Fluid	3.4.4
				Thermal Shock	3.5.1
				Thermal Cycling	3.5.2
				Vibration	3.5.3
				Mechanical Shock	3.5.4
ANSI/J-STD-003	Solderability Tests for Printed Boards	Apr 92	4.3.1	Solderability	3.1.3
ASTM D 635-91	Standard Test Method for Rate of Burning and/or Extent and Time of Burning of Self-Supporting Plastics in a Horizontal Position	Jul 91	All	Flame Resistance	3.2.4
ASTM D 1005-95	Standard Test Method for Measurement of Dry-Film Thickness of Organic Coatings Using Micrometers	Apr 95	All	Coating Thickness	3.2.1
ASTM D 1141-95	Standard Specification for Substitute Ocean Water	Feb 90	All	Sulfur Dioxide/Salt Fog Resistance	3.4.7

(Table 48 continued on next page)

Table 48. Reference Documents (Continued)

Reference Document	Title	Date	Applicable Section(s) of Reference Document	JTP Topic	JTP Section
ASTM D 3359-95a	Standard Test Methods for Measuring Adhesion by Tape Test	Dec 95	Method B	Adhesion Coating Adhesion	3.2.11 4.1.1
ASTM G 21-90	Standard Practice for Determining Resistance of Synthetic Polymeric Materials to Fungi	Oct 90	All	Fungus Resistance	3.2.2
ASTM G 85-85	Standard Practice for Modified Salt Spray (Fog) Testing	Mar 90	All	Sulfur Dioxide/Salt Fog Resistance	3.4.7
Engelmair	The Use Environments of Electronic Assemblies and Their Impact on Surface Mount Solder Attachment Reliability	Jan 90	All	Accelerated Life	3.4.6
FED-STD-141C	Paint, Varnish, Lacquer and Related Materials: Methods of Inspection, Sampling and Testing, Flexibility	Jan 86	Method 6221	Flexibility	3.2.3
IPC-6011	Generic Performance Specification for Printed Boards	Jul 96	All	Current Specifications	1.2
IPC-6012	Qualification and Performance Specification for Rigid Printed Boards	Jul 96	All	Current Specifications	1.2

(Table 48 continued on next page)

Table 48. Reference Documents (Continued)

Reference Document	Title	Date	Applicable Section(s) of Reference Document	JTP Topic	JTP Section
IPC-2221	Generic Standard on Printed Board Design	Not Dated	All	Current Specifications	1.2
IPC-2222	Sectional Design Standard for Rigid Organic Printed Boards	Not Dated	All	Current Specifications	1.2
IPC-9201	Institute for Interconnecting and Packaging Electronic Circuits Surface Insulation Resistance Handbook	Aug 96	6.2.4.3	Modified IPC-B-24 Board	2.1.2
IPC-TM-650	Institute for Interconnecting and Packaging Electronic Circuits Test Methods Manual, Ionic Analysis of Circuit Boards, Ion Chromatography Method	Jan 95	Method 2.3.28	Contamination Characterization	3.1.4
IPC-TM-650	Institute for Interconnecting and Packaging Electronic Circuits Test Methods Manual, Surface Insulation Resistance, Fluxes	Jan 95	Method 2.6.3.3	SIR Environmental 85°C/85% Relative Humidity	3.1.1, 4.1.2 3.4.1
IPC-TM-650	Institute for Interconnecting and Packaging Electronic Circuits Test Methods Manual, Resistance to Electromigration, Polymer Solder Mask	Aug 87	Method 2.6.14	Electromigration	3.1.2

(Table 48 continued on next page)

Table 48. Reference Documents (Continued)

Reference Document	Title	Date	Applicable Section(s) of Reference Document	JTP Topic	JTP Section
IPC-TR-476	Institute for Interconnecting and Packaging Electronic Circuits, How to Avoid Metallic Growth Problems on Electronic Hardware	1977	All	IPC-B-25 Board	2.1.4
MIL-E-5400	General Specification for Aerospace Electronic Equipment	Aug 92	All	Branch Water (Condensed Moisture)	3.4.5
MIL-I-46058C	Insulating Compound, Electrical (for Coating Printed Circuit Assemblies)	Sep 93	All	MIL-I-46058 Y-coupon Type GF Laminate Strip Resonance Thermal Shock Dielectric Withstanding Voltage Insulation Resistance Moisture Resistance Thermal-Humidity Aging Sulfur Dioxide/Salt Fog Resistance	2.1.3 2.1.7 3.2.5 3.2.6 3.2.7 3.2.8 3.2.9 3.2.10 3.4.7
MIL-PRF-38535D	General Specification for Integrated Circuits (Microcircuits) Manufacturing	Apr 96	Table H-IIB	Environmental 85°C/85% Relative Humidity	3.4.1
MIL-STD-202F	Test Methods for Electronic and Electrical Component Parts, Moisture Resistance	Jun 90	Method 106	Moisture Resistance	3.2.9

(Table 48 continued on next page)

Table 48. Reference Documents (Continued)

Reference Document	Title	Date	Applicable Section(s) of Reference Document	JTP Topic	JTP Section
MIL-STD-202F	Test Methods for Electronic and Electrical Component Parts, Thermal Shock	Mar 84	Method 107G	Thermal Shock	3.2.6
MIL-STD-202F	Test Methods for Electronic and Electrical Component Parts, Dielectric Withstanding Voltage	Feb 56	Method 301	Dielectric Withstanding Voltage	3.2.7
MIL-STD-202F	Test Methods for Electronic and Electrical Component Parts, Insulation Resistance	Feb 56	Method 302	Insulation Resistance	3.2.8
MIL-STD-781D	Reliability Testing for Engineering Development, Qualification, and Production	Oct 86	4.3.1.3	Thermal Cycling	3.5.2
MIL-STD-810E	Environmental Test Methods and Engineering Guidelines	Jul 95	Method 507.3	Branch Water (Condensed Moisture)	3.4.5
MIL-STD-810E	Test Method Standard for Environmental Engineering Consideration and Laboratory Tests, Vibrational	Jul 89	Method 514.4	Vibration	3.5.3
MIL-STD-810E	Test Method Standard for Environmental Engineering Consideration and Laboratory Tests, Shock	Jul 89	Method 516.4	Mechanical Shock	3.5.4
MIL-STD-883E	Test Method Standard Microcircuits, Moisture Resistance	Aug 87	Method 1004.7	Condensing Atmosphere	3.4.2

(Table 48 continued on next page)

Table 48. Reference Documents (Continued)

Reference Document	Title	Date	Applicable Section(s) of Reference Document	JTP Topic	JTP Section
MIL-STD-883E	Test Method Standard Microcircuits, Temperature Cycling	May 87	Method 1010.7	Thermal Shock	3.5.1
QPL-46058-75	Qualified Products List of Products Qualified Under Military Specification MIL-I-46058 Insulating Compound, Electrical (for Coating Printed Circuit Assemblies)	Dec 96	All	Conformal Coating Screening Tests	2.4
SAE J1211	Recommended Environmental Practices for Electronic Equipment Design	Nov 78	4.4 4.4	Fluid Exposure –Diesel Fuel Fluid Exposure – Hydraulic Fluid	3.4.3 3.4.4

APPENDIX A

Participating CCAMTF Organizations and Representatives

Table A-1. Participating CCAMTF Organizations and Representatives

Organization	Representative	OEM Type
Alliant Techsystems	Mark Shireman, (612) 931-6506	Military
Allied Signal - Kansas City Division	Gary Becka, (816) 997-4542	Government
Boeing	Willy Chang, (253) 657-9194	Commercial
Contamination Studies Laboratory, Inc.	Terry Munson, (765) 457-8095	Commercial
Electronic Manufacturing Productivity Facility	Mike Czajkowski, (610) 828-8100	Military
Hughes Space & Communication	Tom Carroll (310) 334-4757	Military
GTE	Bill Hubbard, (508) 880-1793	Military
Hanscom AFB	Chuck Bowers (617) 377-8143 Tom Thornton (617) 377-8138	Military
Honeywell	Tom Lepsche, (505) 828-5396	Military
Les Hymes Associates	Les Hymes, (541) 687-0011	Commercial
Lucent Technologies	George Wenger, (609) 639-2769 Bruce Stacy, (908) 582-4289	Commercial
Lockheed Martin Electronics and Missiles	John Lampe, (407) 356-7103 Linda Dolan, (407) 356-2520	Military
Lockheed Martin Tactical Aircraft Systems	Tony Phillips, (817) 777-3758 Charles Palermo, (817) 777-4014	Military
Motorola	Prasad Godavarti, (512) 933-7636	Commercial
Robisan Laboratory	Susan Mansilla, (317) 353-6249	Commercial
Rockwell Collins	David Hillman, (319) 295-1615	Military
Southwest Technology Consultants	Ronald L. Iman, (505) 856-6500	Commercial

(Table A-1 continued next page)

Table A-1. Participating Organizations and Representatives (Continued)

Organization	Representative	OEM Type
Raytheon Systems Company	Jeffry F. Koon, (972) 952-4434 Samantha Walley, (310) 334-3794 Jim Reed, (512) 250-7172 Mike Leake, (972) 334-2071 Jeff Bradford, (972) 952-2170 Mahendra Gandhi, (310) 616-3151 Fonda Wu, (310) 334-3636	Military
US Army - AMCOM, Huntsville	David Carlton, (205) 876-9744	Military
US Army - Picatinny	Larry Genereux, (201) 724-7319	Military
ViaSystems	Lee Parker, (804) 226-5402	
Wright-Patterson AFB	Max Delgado, (937) 255-3059 X329	Military

APPENDIX B

Low Residue Soldering Task Force (LRSTF)
Printed Wiring Assembly (PWA)

B.1 DESIGN OF THE LOW RESIDUE SOLDERING TASK FORCE (LRSTF) PRINTED WIRING ASSEMBLY

The primary test vehicle used in the LRSTF evaluation of low-residue technology was an electrically functional printed wiring assembly (PWA). This assembly was designed at Sandia National Laboratories in Albuquerque, NM based on input from LRSTF members and input received during open review meetings held by the task force.

The PWA measures 6.05 inches x 5.8 inches x 0.062 inches and is divided into seven sections, each containing one of the following types of electronic circuits:

- High Current, Low Voltage (HCLV)
- High Voltage, Low Current (HVLC)
- High Speed Digital (HSD)
- High Frequency Low Pass Filter(LPF)
- High Frequency Transmission Line Coupler (TLC)
- Other Networks (ON)
- Stranded Wire (SW).

The layout of the LRSTF functional assembly is shown in Figure B-1. Each quadrant of the PWA has subsections for PTH and SMT components, with each forming separate electrical circuits. The PWA includes a large common ground plane, components with heat sinks, and mounted hardware.

Each subsection shown contains both functional and nonfunctional components (added to increase component density). A 29-pin PTH edge connector is used for circuit testing. High frequency connectors are used to ensure proper impedance matching and test signal fidelity as required. Board fabrication drawings, schematics, and a complete listing of all components are available in separate cover.

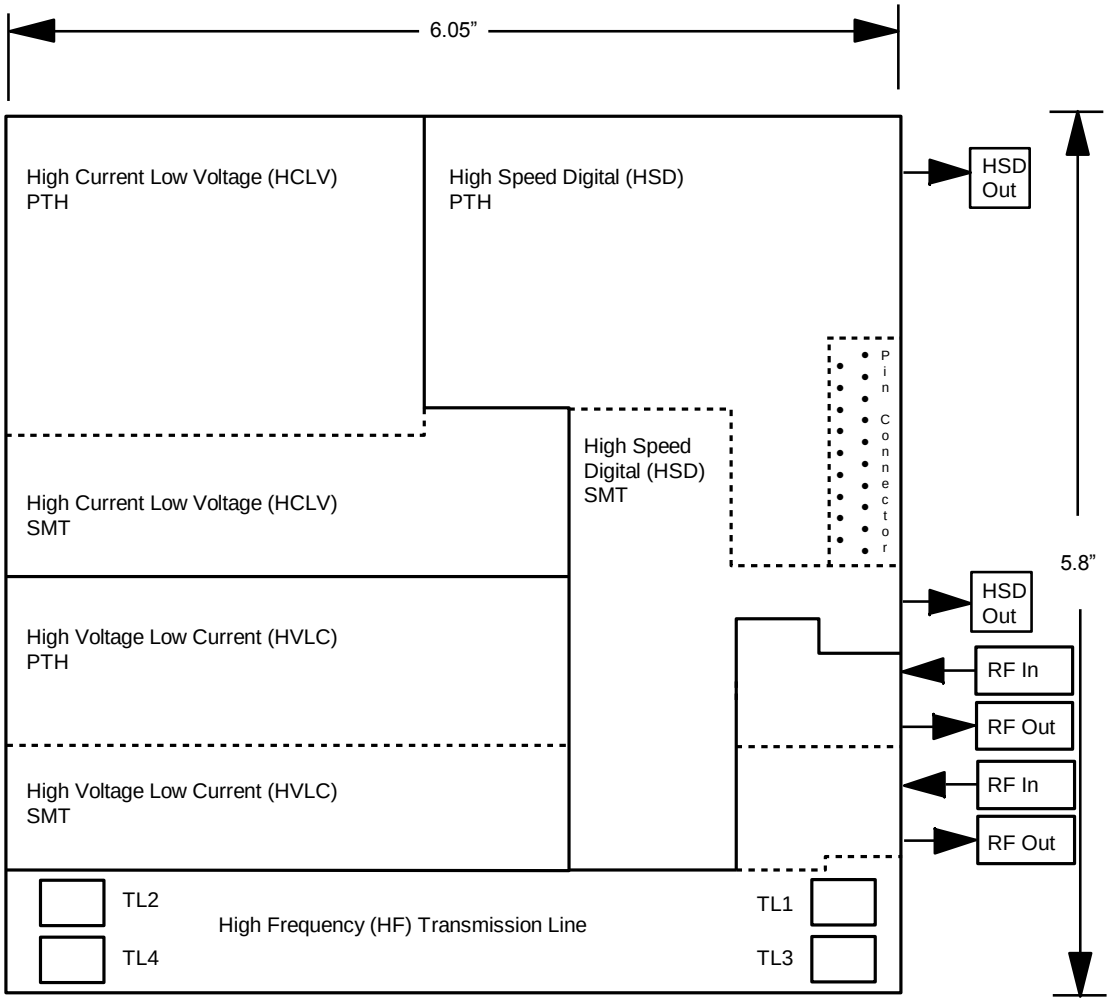


Figure B-1. Layout of the PWA Illustrating the Four Major Sections and Subsections

B.2 HIGH CURRENT, LOW VOLTAGE (HCLV)

The HCLV section of the board is in the upper left-hand corner of LRSTF PWA (see Figure B-1). The upper left-hand portion of this quadrant contains PTH components with SMT components immediately beneath.

Purpose of the HCLV Experiment

Performance of high-current circuits is affected by series resistance. Resistance of a conductor (including solder joints) is determined by the following equation:

$$R = \frac{\rho L}{A_c} ohms(\Omega) \qquad \text{(B.1)}$$

where ρ = resistivity, the proportionality constant
L = length of the conductor
A_C = cross-sectional area of the conductor (solder joints).

Resistance is most likely to change due to cracking or corrosion of the solder joint that may be related to the soldering process. These conditions decrease the cross-sectional area of the solder joints, thus increasing resistance as shown in Equation B.1. Use of high current to test solder joint resistance makes detection of a change in resistance easier. A 5 Amperes (A) current has been selected as a value that would cover most military applications. A change of resistance is most conveniently determined by measuring the steady-state performance of the circuit, which will now be discussed.

Steady State Circuit Performance.

Overall circuit resistance, R_{total}, is the parallel combination of the seven resistors, R_1, R_2, ..., R_7, (all resistors = 10Ω) used in the HCLV circuit:

$$\frac{1}{R_{total}} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_2} + \cdots + \frac{1}{R_7} = \frac{7}{10\Omega} \qquad \text{(B.2)}$$

$$R_{total} = \frac{10\Omega}{7} \qquad \text{(B.3)}$$

Since a current (I) of 5A will be applied to the circuit, the resulting voltage (V), according to Ohm's Law, is:

$$V = IR = 5A \times \frac{10\Omega}{7} = 7.14V \qquad \text{(B.4)}$$

Changes in resistance are thus detected by changes in voltage. However, a pulse width had to be chosen that would not overstress the circuit components. With current equally

divided among the seven parallel resistors, the power (P) dissipated in each resistor, according to Joule's Law, is:

$$P = I^2 R = \left(\frac{5A}{7}\right)^2 \times 10\Omega = 5.1 Watts(W) \qquad \text{(B.5)}$$

Since the power rating for the PTH wire-wound resistor is 3W, the rating is exceeded by a factor of 1.7 for steady state (5.1 / 3). Design curves from the resistor manufacturer indicate the PTH wire-wound resistors could tolerate the excess power for about 100 *ms*. The SMT resistors are rated at 1W, so the steady state rating is exceeded by a factor of five. With the manufacturer unable to provide the pulse current capability of the SMT resistors, a pulse derating factor could not be determined. A pulse width of 100 μ*s* was selected, which is three orders of magnitude less than the capability of the wire-wound resistors. This width is also sufficiently long for the circuit to achieve steady state before the measurement is taken.

Circuit Board Design

Traces carrying the 5A current were placed on an inner layer of the circuit board because: (1) the primary concern was the possible degradation of the solder connections as discussed above, and (2) the bulk electrical characteristics (resistivity) of the traces should not be affected by flux residues. High-current trace widths were designed to be 250 mils whenever possible (following MIL-STD-275). This width with a 5A current should cause no more than a 30°C temperature rise under steady-state conditions.

The resistor and capacitor values were selected to be readily available. If other values are used, care should be taken to not over-stress the parts, as discussed above.

B.3. HIGH VOLTAGE LOW CURRENT

The HVLC circuitry is immediately below the HCLV circuitry and above the high-frequency transmission lines. The PTH circuitry is in the upper part of this subsection with the SMT circuitry beneath.

Purpose of the HVLC Experiment

Flux residues could decrease the insulation resistance between conductors. The impact of this decrease could be significant in circuits with a high-voltage gradient across the insulating region. Decreased resistance can be detected by an increase in current when a high voltage is applied to the circuit. A voltage of 250V was selected as the high potential for this test. The change in leakage current is determined by measuring the steady-state performance of the circuit, which will now be discussed.

Steady State Circuit Performance

Steady-state operation of the HVLC circuit can be determined by considering only the resistors. The total resistance of the series combination is the sum of the resistances:

$$R_{total} = R_1 + R_2 + R_3 + R_4 = R_5 = 50\,M\Omega \qquad \text{(B.6)}$$

since all resistors are 10MΩ each.

From Ohm's law, the current flowing into the circuit with 250V applied is:

$$I = \frac{V}{R} = \frac{250V}{50\,M\Omega} = 5\mu A \qquad \text{(B.7)}$$

Care was taken to not over-stress the individual components in the circuits. The voltage stress across each resistor-capacitor pair is one-fifth of the applied 250V, or 50V. The voltage ratings are 250V for the PTH resistors, 200V for the SMT resistors, and 250V for all the capacitors. Power rating is not a concern due to the low current.

Circuit Board Design

High voltage traces were placed next to ground potential traces by design. The spacings between the high voltage and intermediate traces were selected using MIL-STD-275 and were calculated as shown in Table B-1 below.

Table B-1. Voltage per Trace Spacing

Voltage	Spacing Between Traces (mils)
0 - 100	5
101 - 300	15
301 - 500	30

These guidelines were followed except the 5-mil spacing, where 10 mils was used to facilitate board fabrication. Table B-2 lists the voltage on various board circuit traces and the spacing to the adjacent ground trace.

Resistors and capacitors were selected to have readily available values — different values could have been used to achieve particular experimental goals. For instance, higher-resistance values could be used with lower-value capacitors. Reverse biased, low-leakage diodes could also be used for higher sensitivity to parasitic leakage resistance.

Table B-2. HVLC Circuit Board Trace Potentials

Technology	Trace Connected to:		Potential (V)	Trace Length at Potential (in)	Spacing (mils)
	Resistor	Capacitor			
PTH	R15	C21	250	0.8	30
			200	0.4	15
	R16	C22	200	0.4	15
			150	N/A	
	R17	C23	150	N/A	
			100	0.4	10
	R18	C24	100	0.4	10
			50	N/A	
	R19	C25	50	N/A	
SMT	R20	C26	250	5.0	30
			200	1.0	15
	R21	C27	200	1.0	15
			150	N/A	
	R22	C28	150	N/A	
			100	0.9	10
	R23	C29	100	0.9	10
			50	N/A	
	R24	C30	50	N/A	

N/A = Not Applicable since no 50V or 150V traces were adjacent to ground potential

B.4. HIGH SPEED DIGITAL (HSD)

The HSD circuitry is in the upper right-hand corner of the LRSTF PWA as shown in Figure B-1. This subsection contains the PTH circuitry and consists of two 14-pin dual in-line package (DIP) integrated circuits (ICs). The SMT subsection IC is a single 20-pin leadless chip carrier (LCC) package. Each of these ICs is a "fast" bi-polar digital "QUAD-DUAL-INPUT-NAND-GATE." Both subsections contain two ceramic capacitors that bypass spurious noise on the power input line (VCC) to the ICs and an output high-frequency connector. Inputs to both subsections are applied through the edge-connector on the right side of the board. Figure B-2 shows a simplified schematic of the ICs.

Purpose of the HSD Experiment

The output signal of each gate in Figure B-2 is opposite in polarity to the input signal. If the traces of these two signals are in close proximity on the printed circuit board (capacitively coupled), the gate switching speed might be affected by the presence of flux residues. A 5 VDC bias will be applied to the VCC inputs during environmental testing to accelerate aging. One PTH IC (U02) will be hand soldered during assembly at each site to introduce hand solder flux residue in the experiment.

Circuit Description

The schematic in Figure B-2 represents the ICs in the PTH and SMT subsections. The ICs are random logic circuits that are NAND (Not AND) gates. An AND gate's output is high only when all inputs are high. The logic of a NAND gate is opposite the logic of an AND gate. Therefore, the output of a NAND gate is low only when all inputs are high; otherwise, the output is high. With the two connected inputs, the output of each gate is opposite the input. Since the four gates are connected in series, the output of the last gate is the same logic level (high or low) as the input, with a slight lag.

The output pulse does not change logic levels instantaneously, but the switching times from low to high (rise time) and from high to low (fall time) should be less than 7ns. ICs should perform within these criteria if the VCC input is 5 ± 0.5V DC, the output load does not exceed specifications, and the circuit has a proper ground plane as shown in Figure B-2.

The HSD circuits also provide an intermediate test for high frequencies, with switching time dictating a high-frequency spectrum. The frequency spectrum of switching circuits can be expressed in terms of bandwidth (BW). For a switching circuit, the respective BWs (in Hertz) for rise (t_r) and fall (t_f) times are:

$$BW_r = \frac{0.35}{t_r} Hz \quad and \quad BW_f = \frac{0.35}{t_f} Hz \qquad (B.8)$$

Bipolar technology was used rather than a complementary metal oxide semiconductor (CMOS) since it is not as vulnerable to electrostatic discharge (ESD) damage. Available military bipolar technologies have typical switching speeds and bandwidths as indicated in Table B-3 below.

Table B-3. Typical Switching Speeds and Bandwidths

Technology	Typical t_r or t_f (ns)	Bandwidth (MHz)
5404 TTL	12	29
54LS04 Low Power Schottky	9	39
54S04 Schottky	3	117
54F04 Advanced Schottky (Fast)	2.5	140

The Fast technology was selected since it had the shortest switching time and largest bandwidth, which provides the widest frequency spectrum for this test.

Circuit Board Design

Ground planes were provided for proper circuit operation of the ICs. The PTH subcircuit utilized the large common ground plane on layer 3 since most of the input and output traces are on layer 4. Since the SMT circuit traces are on the top layer, a smaller ground plane was added on layer 2. The "QUAD-DUAL-INPUT-NAND-GATE" was selected since other solder studies of national attention have used that particular type of IC, which makes direct comparisons with these studies possible. See Figure B-2.

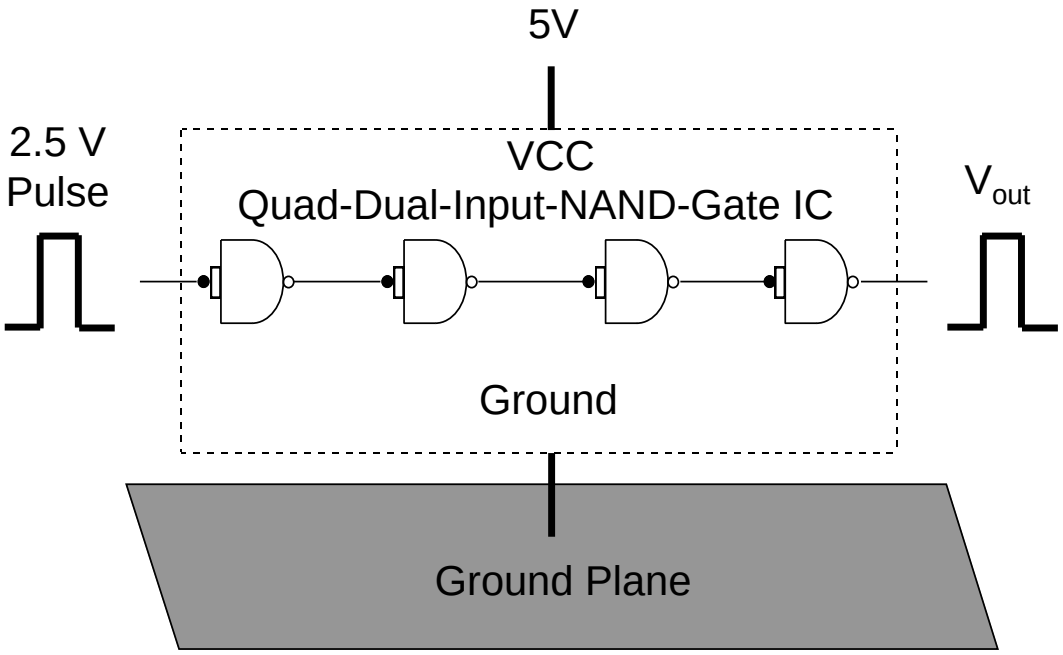


Figure B-2. Simplified Schematic of the ICs in the HSD Subsection

B.5. HIGH FREQUENCY (HF)

The HF section shown in the lower right-hand corner of Figure B-1 contains two major subsections, the low-pass filters (LPF) and the transmission line coupler (TLC). The TLC traces on layer 4 of the board are on the backside of the board. The LPF/PTH subsection is above the LPF/SMT subsection. Each of these subsections has discrete ceramic capacitors and three inductor-capacitor (LC) filters, with the inductor printed on the circuit board in a spiral pattern. The HF circuits allow evaluation of circuit performance up to 1GHz (1 GHz).

Purpose of the High Frequency Experiment

Flux residues may affect the performance of LPF printed circuit inductors and transmission lines due to parasitic resistances and parasitic capacitances. These inductors will be purposely covered with flux during surface-mount solder processing to increase the presence of residues. Since the transmission lines are separated by only 10 mils, flux residues between the lines may affect their performance.

LPF Circuit Description

An inductor-capacitor (LC) LPF consists of a series inductor followed by a shunt capacitor. A low-frequency signal passes through the LPF without any loss since the inductor acts as a short circuit and the capacitor acts as an open circuit for such signals. Conversely, a high-frequency signal is blocked by the LPF since the inductor acts as an open circuit and the capacitor acts as a short circuit for such signals.

When a sine wave test signal is passed through an LPF, its amplitude is attenuated as a function of frequency. The relationship between the output and input voltage amplitudes can be expressed as a transfer function. The transfer function, V_{out} / V_{in}, was measured to determine any effects of the low-residue fluxes.

The transfer function is measured in decibels (dB) as a function of frequency. A decibel can be expressed in terms of voltage as follows:

$$dB = 20\log_{10}\left(\frac{|V_{out}|}{|V_{in}|}\right) \qquad \text{(B.9)}$$

The PTH transfer function differs from the SMT transfer function due to the self inductance of the capacitor through-hole leads.

LPF Circuit Board Design

The three LC LPFs for each of the SMT and PTH circuits were designed to have the following cutoff frequencies: 800, 400, and 200 MHz. Cutoff frequency is that frequency for which the transfer function is -3 dB. The respective component values chosen for the

LC filters are 16 nH (nano-Henries) and 6.4 pF (pico-Farads), 32 nH and 13 pF, and 65 nH and 24 pF. Most LPF circuitry was placed on Layer 1, with Layer 2 used as a ground plane. Crossovers needed to connect the LPF circuits are on Layer 4.

The LPF circuits were designed to operate with a 50Ω test system, so all interconnect traces longer than 0.10 inches were designed as 50Ω transmission lines to avoid signal distortion. The LPF circuits were predicted to have less than 2 dB loss below 150 MHz, approximately 6 dB loss near 235 MHz, and greater than 40 dB loss at 550 MHz and beyond. The measured response of the LPF/SMT circuit is close to that predicted except that the transfer function decreases more rapidly than predicted above 350 MHz . As stated previously, the PTH circuit transfer function did not perform similarly to the SMT, particularly at frequencies above 150 MHz.

TLC Circuit Description

Figure B-3 shows a diagram of the TLC subsection. The LPFs described above are *lumped-element* circuits since the capacitors are discrete components. The TLC lines are *distributed-element* circuits with the resistors, inductors, and capacitors distributed along the lines. A circuit model for the lines is shown in Figure B-4.

The inductance and capacitance for a transmission line with a ground plane are, respectively:

$$L_L = 0.085 R_0 \sqrt{\varepsilon_r}\, nH / in \qquad \text{(B.10)}$$

$$C_L = \frac{85}{R_0} \sqrt{\varepsilon_r}\, pF / in \qquad \text{(B.11)}$$

where R_0 = characteristic resistance and ε_r = dielectric constant of the board material.

The TLC R_o was designed to be 50Ω for operation with a 50Ω test system. For FR-4 epoxy (board substrate material), L_L is about 9.6 nH/in and C_L is about 3.8 pF/in.

The TLC was tested with a sine wave signal similar to the one used in testing the LPFs.

The source resistance was 50Ω and the three output terminals were connected to 50Ω loads.

TLC Circuit Board Design

The transmission line coupler (TLC) circuit has a pair of coupled 50Ω transmission lines with required measurable performance frequencies less than 1 GHz. Layer 4 of the printed wiring board (PWB) was used to route the TLC circuit, with Layer 3 used as the ground plane. The TLC circuit is a 5 inches long pair of 0.034 inches wide 50Ω

transmission lines spaced 0.010 inches apart. The circuit design incorporated the board dielectric constant of about 4.8 inches and the .020 inch spacing between copper layers. A computer-aided circuit design tool (Libra) was used to model the TLC circuit. Performance measured on a test PWB agreed very closely with the forward and reverse coupling predictions between 45 MHz and 1 GHz.

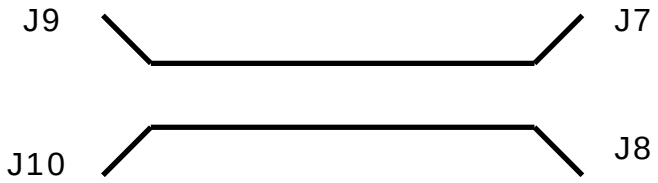


Figure B-3. Diagram of the HF/TLC Subsection

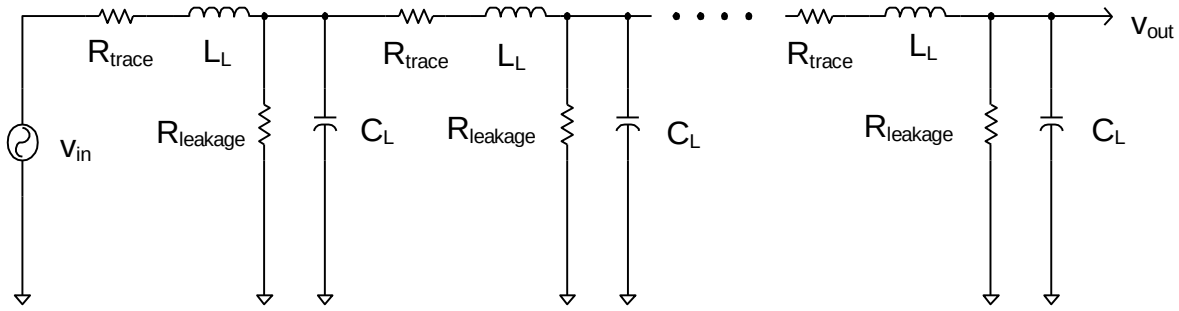


Figure B-4. HF/TLC Distributed Element Model

B.6. OTHER NETWORKS (LEAKAGE CURRENTS)

The LRSTF board also contains three test patterns to provide tests for current leakage: (1) the pin-grid array (PGA), (2) the gull wing (GW), and (3) 10-mil spaced pads. A 5 V source was used to generate leakage currents.

Purpose of the Experiments

The PGA, GW, and 10-mil pads allow leakage currents to be measured on test patterns that are typical in circuit board layouts. These patterns contain several possible leakage paths and the leakage could increase with the presence of flux residues and environmental exposure. In addition, solder mask was applied to portions of the PGA and GW patterns to evaluate its effect on leakage currents and the formation of solder balls.

Pin-Grid Array

The PGA hole pattern has four concentric squares that are electrically connected by traces on the top layer of the board as shown in Figure B-5. The pattern also has four vias just inside the corners of the innermost square that are connected to that square. Four vias were placed inside the innermost square to trap flux residues. Two leakage current measurements were made: (1) between the two inner squares (PGA-A) and (2) between the two outer squares (PGA-B), as shown in Figure B-5. Solder mask covers the holes of the two outer squares on the bottom layer, allowing a direct comparison of similar patterns with and without solder mask.

Rather than an actual PGA device, a socket was used since it provided the same soldering connections as a PGA device. Also, obtaining leakage measurements on an actual PGA is nearly impossible due to complexity of its internal semiconductor circuits.

Gull Wing

The upper half of the topmost GW lands and the lower half of the bottom most GW lands were covered with solder mask to create a region that is susceptible to the formation of solder balls. The lands were visually inspected to detect the presence of solder balls. A nonfunctional GW device is installed with every other lead connected to a circuit board trace forming two parallel paths around the device. Total leakage current measurements were made on adjacent lands of the GW device

10-mil Pads

The 10-mil pads were laid out in two rows of five pads each. The pads within each row were connected on the bottom layer of the board and leakage between the rows was measured.

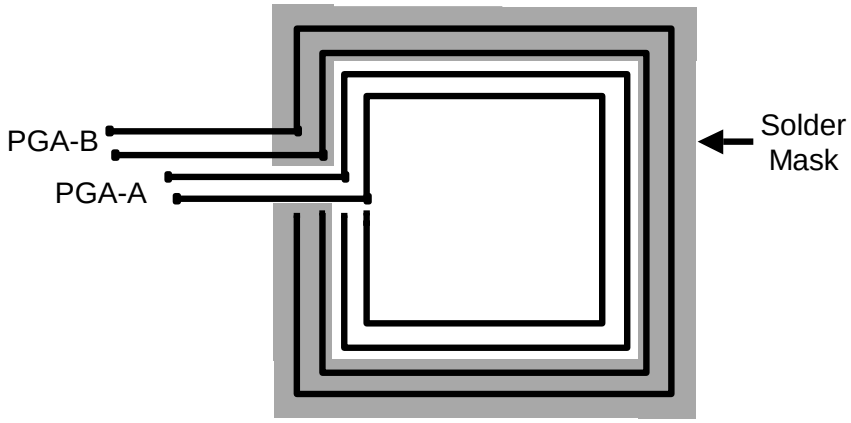


Figure B-5. PGA Hole Pattern with Solder Mask

B.7. STRANDED WIRES

Two 22-gauge stranded wires will be hand soldered just to the left of the edge connector. One wire will be soldered directly into the board through holes and the other will be soldered to two terminals, E17 and E18. Each wire is 1.5 inches long, is silver coated, and has white PTFE insulation. All wires will be stripped, tinned, and cleaned in preparation for the soldering process.

Purpose of the Stranded Wire Experiment

Stranded wires were used to evaluate flux residues and subsequent corrosion.

Circuit Description

The 5 A 100 μs pulse used to test the HCLV circuit was injected into each of the stranded wires for electrical test. A separate PWB trace was connected to each end of the stranded wire. Test wires were connected to the separate traces allowing to provide the means to measure the voltage drop across the stranded wires. In this manner, the voltage drop was measured independently from any voltage drop in the test wires conducting the 5 A pulse to the stranded wires.

B.8. COMPONENTS

All functional component types conformed to commercial specifications and were ordered pre-tinned (to the extent possible). Components will not pre-cleaned before use.

Solderability testing will be performed using dip and look testing per MIL-STD-202, Method 208 with type R flux per MIL-F-14256. All functional components are required to pass solderability testing.

B.9. BOARDS

The four-layer LRSTF PWBs have exposed traces on both sides and will be manufactured to meet the requirements of MIL-P-55110. The substrate material will be FR-4 epoxy. Starting copper weight will be 1 oz/ft^2. An ionic cleanliness level of 5 or less μg/in^2 NaCl equivalence will be specified.

Figure B-6. LRSTF Functional Test Board

APPENDIX C

Circuit Card Assembly and Materials
Task Force Automated Test Set

C.1. CCAMTF AUTOMATED TEST SET

The CCAMTF Automated Test Set (ATS) is used to perform automatic testing of the Low-Residue Soldering Task Force (LRSTF) printed wiring assembly (PWA). The Automated test set design was based on the original LRSTF manual test setup. The CCAMTF ATS was designed to emulate the LRSTF manual test set as much as possible. Some changes were made in the selection of commercial test equipment in order to facilitate the test software development process. Some test stimuli and test measurement techniques were also changed in order to be compatible with the commercial test equipment selected. See figure C-1.

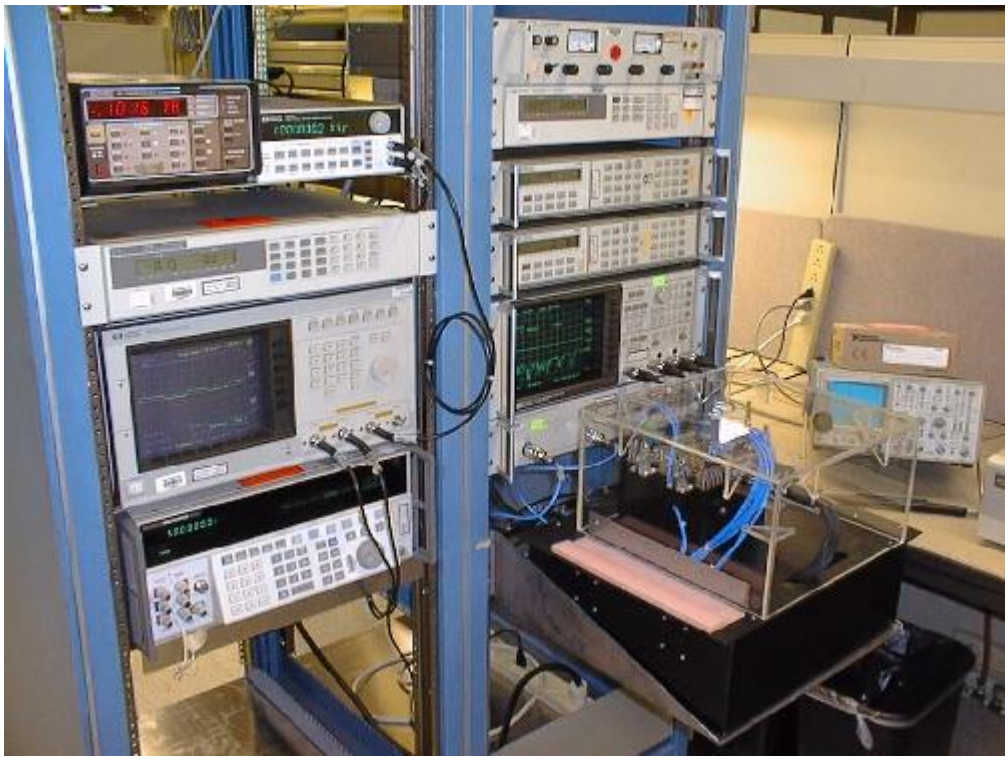


Figure C-1. CCAMTF Automated Test Set

Table C-1. CCAMTF ATS Commercial Test Equipment

Test Equipment	Description
Hewlett Packard HP6289A	Power Supply
Hewlett Packard HP8112A	Pulse Generator
Hewlett Packard HP54111D	Digital Oscilloscope
Hewlett Packard HP6060B	Electronic Load
Hewlett Packard HP3488A	Switch/Control Unit (2 each)
Hewlett Packard HP44471A	General Purpose Relay (3 each)
Hewlett Packard HP44472A	VHF Switch(2 each)
Hewlett Packard HP44470A	10 Channel Relay Multiplexer
Hewlett Packard HP85046A	S - Parameter Test Set
Hewlett Packard HP8753A	Network Analyzer
Fluke 5700A	Voltage Calibrator
Keithley 617	Electrometer

The commercial test equipment is housed in a two bay cabinet. Signal routing and switching are performed by the HP3488 Switch/Control units. Custom designed interconnect cables are used to make the connections between the commercial test equipment, the switch/control units and the PWA under test. All commercial test equipment is connected to the computer using standard GPIB interconnect cables.

C.2. PWA TEST FIXTURE ASSEMBLY

The PWA Test Fixture Assembly contains interconnect wiring that provides electrical connection between the PWA under test and the commercial type test equipment as shown in Figure C-2 CCAMTF Automated Test Set PWA Test Fixture Assembly.

The PWA under test is mounted horizontally in the test fixture to facilitate the connection of RF coaxial cables. A cable harness is connected to the PWA edge card connector. Ejectors are provided to assist in the connector mating and de-mating. Two microwave coaxial switches are mounted in the base of the fixture. There are no other active components in the test fixture.

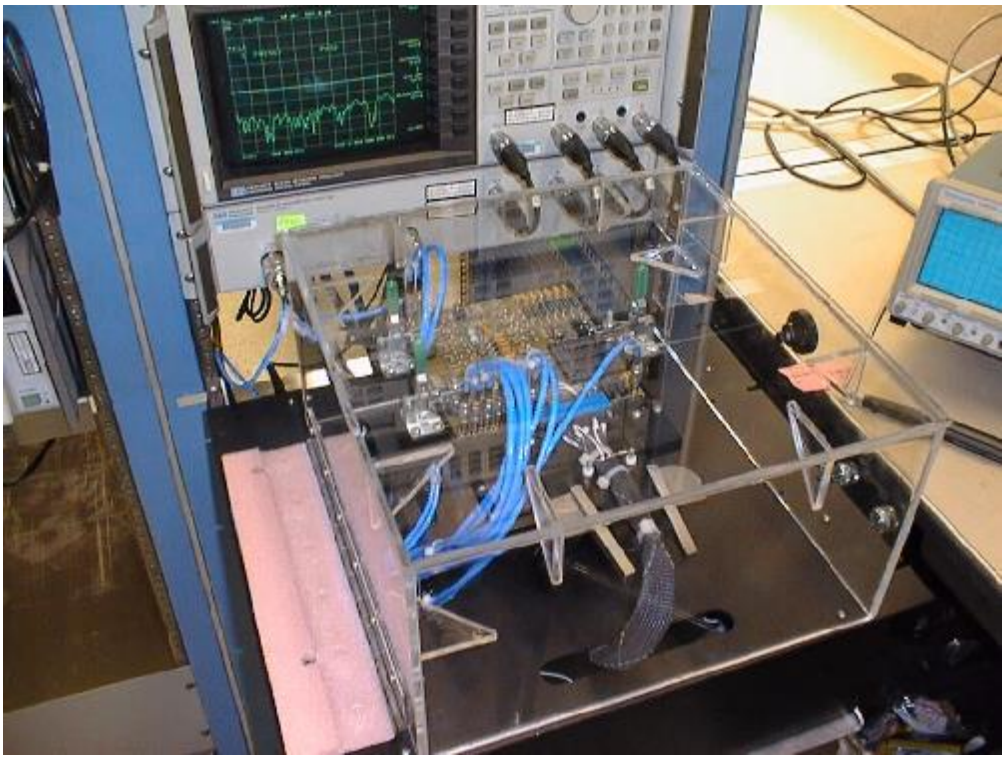


Figure C-2. CCAMTF Automated Test Set PWA Test Fixture Assembly

Two microwave switches provide signal switching for high frequency type measurements. One switch directs signals to the PWA inputs and the second switch selects the corresponding outputs that are routed to the measurement equipment. The coaxial switches are controlled by the computer and the test software. Coaxial cable insertion losses are measured during the ATS calibration procedure. Cable losses are recorded and subtracted from the PWA test measurements to arrive at the actual PWA insertion losses.

A plexiglas cover is provided to shield the operator from exposed high voltage on the PWA. An interlock switch is installed on the cover. Opening the cover will disconnect the high voltage from the PWA. Connections are provided on the plexiglas cover to attach a three inch flexible air hose. The air hose is connected to a facility exhaust system to prevent diesel and hydraulic fluid fume build up during the fluids testing procedure. The air hose connection is required only during the fluids test.

C.3. TEST SOFTWARE

An IBM compatible computer running the Windows operating system is used to control the test sequence and record test measurement results. Windows is a product of Microsoft Corporation, Portland, OR. A National Instrument GBIP Interface card is installed in the computer to interface with the commercial test equipment.

Test Executive (TEXEC) is a software system used to control test selection, test execution, and test data output. TEXEC is a product of Serendipity Systems, Inc. (SSI) of Sedona, AZ.

Lab Windows/CVI is a visual programming tool used to develop test software. Lab Windows/CVI is a product of National Instruments of Austin, TX.